背景资料

Intel Technology and Manufacturing Day Glossary
英特尔精尖制造技术词汇表

- **cell height** – The logic cells in a cell library are rectangular and designed with a fixed height so they can be placed side by side in parallel rows, and readily interconnected. The cell height is the thickness of these rows.
- **单元高度** – 单元库中的逻辑单元是矩形并且以固定高度设计的，以便可以将它们并排放置于平行的行中且易于互连。单元高度就是这些行的厚度。

- **cell library** – A library (collection) of hundreds of logic cells such as the NAND2. A designer chooses specific cells and connects them in a specific manner to form a logic circuit – an adder is an example – part of a chip design.
- **单元库** – 包含数百个逻辑单元（如 NAND2）的库（集合）。设计师选择特定的单元，并以特定的方式连接它们，从而形成逻辑电路例如加法器，为芯片设计的一部分。

- **COAG (contact over active gate)** – A process feature whereby the gate contact is stacked on top of the transistor gate rather than at its side. Intel has implemented COAG in its 10nm process – an industry first – thereby improving transistor density.
- **COAG（有功栅极上触点）**– 栅极触点堆叠在晶体管栅极上方而不是在其侧面的一种工艺特性。英特尔是业内首创在其 10 nm 制程中使用了 COAG 来提高晶体管密度。

- **CPT (cost per transistor)** – The cost of building a single transistor, calculated as the number of transistors that can be manufactured on a wafer divided by the cost of processing a single wafer. Perhaps the most important benefit of Moore's Law is the steady reduction in CPT, thereby delivering ever more value to the end user.
- **单个晶体管成本（CPT）** – 制造单个晶体管的成本，由一个晶圆上可制造的晶体管数量除以处理单个晶圆的成本计算所得。也许摩尔定律最重要的益处就是单个晶体管成本的稳步下降，从而给最终用户带来了更高的价值。

- **contact** – A conductor that connects one of the terminals of a transistor to a metal layer. Contacts are usually created from tungsten.
- **触点** – 将晶体管的一个极连接到金属层的导体。触点通常由钨制成。

- **double patterning or LELE** – The use of two steps (LELE = litho-etch-litho-etch) to create the desired pattern on one layer. Double patterning is required when the wavelength of the lithography tool (scanner) doesn't provide sufficient resolution to

create the desired feature sizes. The LELE process has yield and performance risk from misalignment between patterns.

- **双图案成形或双微影蚀刻（LELE）** – 使用两个步骤（双微影蚀刻=光刻-蚀刻-光刻-蚀刻）在单层上创建所需的图案。当光刻工具（扫描仪）的波长提供的分辨率不足，无法产生期望的特征尺寸时，需要使用双图案成形。由于图案之间对不齐，双微影蚀刻工艺有存在良品率和性能风险。

- **dummy gate** – A gate that isn't part of a transistor, put on the edge of a logic cell, needed to isolate one cell from another. Traditional processes used two dummy gates per cell; Intel's 10 nm process requires only a single dummy gate, thereby improving transistor density.
- **虚拟栅极** –一个放置在逻辑单元的边缘将单元与单元隔离，但不属于晶体管的栅极。传统工艺每个单元使用两个虚拟栅极；英特尔的 10nm 工艺只需要一个虚拟栅极，从而提高了晶体管的密度。

- **FinFET (aka tri-gate transistor)** – Introduced by Intel in 2011, it is a transistor structure whereby the gate wraps around the channel (the region where current flows from source to drain), which is in the shape of one or more vertical fins. This improves performance and reduces power over the traditional planar transistor in which the gate controls channel flow only from above.
- **FinFET（鳍式场效应晶体管，又称三栅极晶体管）** – 由英特尔于 2011 年推出，这是一种晶体管结构，其栅极围绕通道（电流从源极到漏极的区域），形状为一个或多个垂直鳍。 这和传统平面晶体管比较提高了性能并降低了功耗。在传统平面晶体管中，栅极只从上方控制通道电流。

- **high-k metal gate** – A technique adopted by Intel in 2007 for reducing transistor leakage (wasted power) while increasing transistor performance, allowing transistor scaling to continue in accordance with Moore's Law. The solution was to replace the transistor's silicon dioxide gate dielectric (a thin layer below the gate) with a hafnium-based "high-k" material.
- **高 k 金属栅极** – 英特尔在 2007 年采用的一项技术，用于在提高晶体管性能的同时减少晶体管漏电（浪费的功耗），让晶体管继续按照摩尔定律缩小。该解决方案以基于铪的"高 k"材料代替晶体管的二氧化硅栅极电介质（栅极下方的薄层）。

- **logic cell** – Logic cells contain a small number of transistors connected together to form a simple binary logic or storage function. A simple example is a NAND2 cell, which is built with four transistors. It has two inputs and one output. Each input can be a zero or one (zero is represented by low voltage, one by high voltage). If both inputs are one, then the output is zero. If one or both inputs is zero, the output is one. Logic circuits are built by combining logic cells.
- **逻辑单元** – 逻辑单元包含少量连接在一起的晶体管，形成简单的二进制逻辑或存储功能。一个简单的例子是一个 NAND2 单元，它由四个晶体管构成，有两个输入和一个输出。每个输入可以是一个 0 或者一个 1（0 由低电压表示，1 由高电压表示）。如果两个输入均为 1，则输出为 0。 如果一个或两个输入为 0，则输出为 1。 逻辑电路是通过逻辑单元的组合来构建的。

- **metal, interconnect** – An integrated circuit consists of a large number of transistors

whose three terminals (source, drain and gate) are connected together in a very specific fashion by conducting interconnects (electrical wires). These interconnects are made of metal and sometimes referred to simply as “metal.” The most common metal used for this purpose is copper.

- **金属，互连线–** 集成电路由大量晶体管组成，其三个极（源极、漏极和栅极）通过导电的互连线（电线）非常特定的方式连接在一起。这些互连线由金属制成，有时简称为“金属”。用于此目的的最常见金属是铜。

- **Mtr/mm2** – The unit for transistor density. Measures how many million transistors can be packed into an area 1 mm by 1 mm.
- **Mtr/mm2 （百万晶体管/平方毫米）–**每平方毫米晶体管数量（单位：百万），这是晶体管密度单位。测量 1mm×1mm 的区域可以容纳多少百万个晶体管。

- **nm** – Nanometer, one-billionth of a meter. It takes only four silicon atoms in a crystal lattice to make one nanometer.
- **nm –** 纳米，十亿分之一米。晶格中只需四个硅原子就会达到 1 纳米。

- **patterning** – The process of creating a layer of material on a wafer in a specific pattern. The most common way to do so is to cover the wafer with a photoresist (light-sensitive material), shine light through a patterned mask onto the wafer to expose desired portions, then etch away the exposed resist, leaving a particular pattern on the wafer.
- **图案成形 –** 以特定图案在晶圆上形成材料层的过程。最常见的方法是用光致抗蚀剂（感光材料）覆盖晶圆，让光通过图案化掩模版（mask）照射到晶圆上以露出所需部分，然后蚀刻掉曝光后的抗蚀剂，在晶圆上留下特定图案。

- **pitch** – A measure of how closely spaced a linear feature can be in a particular process. For instance, in Intel’s 14 nm process, interconnects placed together side by side have a 52 nm pitch, meaning the sum of the minimum width and the minimum spacing is 52 nm.
- **间距 –**在特定制程工艺中线性特征间隔多少的一种度量。例如，在英特尔的 14nm 制程中，并排放置的连接线具有 52nm 的间距，意味着最小宽度和最小间隔之和为 52nm。

- **SADP (self-aligned double patterning)** – A patterning technique that uses a spacer material to create features with half the original lithographic pitch. It allows better pitch scaling than LELE while adjacent lines are kept self-aligned to each other.
- **SADP（自校准双图案成形）–** 运用间隔材料创造具有原始光刻间距一半特征的图案成形技术。它可以使相邻的线条保持彼此自动相互校准，实现比双微影蚀刻（LELE）更好的间距缩小。

- **SRAM cell** – A high-speed memory cell, built into arrays, used in logic chips for registers and caches, for temporarily storing data on a processor. It typically contains six transistors. As today’s processors tend to have very large caches, an important consideration in the design of new processes is to minimize the SRAM cell size.
- **SRAM（静态随机存取存储器）单元–** 内置于阵列中的高速存储器单元，在逻辑芯片中用于寄存器和缓存，把数据临时存储在处理器上。通常包含六个晶体管。由于现今的处理器往往具有非常大的缓存，因此新制程设计中的一个重要考虑因素是尽量缩小 SRAM 单元的尺寸。

- **strained silicon** – A technique adopted by Intel in 2003 for speeding up transistors by creating a compressive strain for PMOS transistors and a tensile strain for NMOS transistors, increasing current flow when a transistor is in the “on” state.
- **应变硅** – 英特尔于 2003 年采用的一种技术，通过为 PMOS 晶体管（正极金属氧化物半导体）产生压缩应变和为 NMOS 晶体管（负极金属氧化物半导体），在晶体管处于“导通”状态时增加电流，产生拉伸应变来提升晶体管速度。

- **transistor** – A tiny switch that controls the flow of electricity. It is the fundamental building block of logic circuits. There are two types, NMOS and PMOS (negative and positive metal oxide semiconductors). The transistor has three terminals: source, drain and gate. In an NMOS transistor, current flows from the source to the drain only when the gate is at high voltage; in a PMOS transistor, current flows only when the gate is at low voltage. NMOS and PMOS are complementary, making today’s CMOS processes.
- **晶体管** – 控制电流的微型开关。它是逻辑电路的基本构建模块。有 NMOS（负极金属氧化物半导体）和 PMOS（正极金属氧化物半导体）两种类型。晶体管有三个极：源极、漏极和栅极。在 NMOS 晶体管中，只有当栅极处于高电压时，电流才从源极流到漏极；在 PMOS 晶体管中，只有当栅极处于低电压时，电流才会流动。NMOS 和 PMOS 互补，形成了目前的 CMOS（互补金属氧化物半导体）工艺。

- **transistor performance, drive current** – The performance of a transistor – how fast it can switch from off to on, or vice versa – is proportional to the amount of current that it drives from its drain. An important consideration in the design of a new process is to increase drive current and to reduce power per transistor. Drive current is a factor in determining the maximum frequency at which a chip can run.
- **晶体管性能，驱动电流** – 晶体管的性能即开/关切换的速度，与其从漏极驱动的电流量成正比。 设计新制程的一个重要考虑因素是增加驱动电流并降低每个晶体管的功耗。驱动电流是决定芯片最大运行频率的一个因素。

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