LC717A00AR

电容数字转换器LSI (适用于静电电容式触摸传感器)

概述

LC717A00AR是一款高性能、低成本的电容数字转换器LSI，适用于静电电容式触摸传感器，尤其注重可用性。这款产品拥有8信道电容传感器输入。内置逻辑电路可检测各输入的(开/关)状态，并输出结果。这使其成为各种开关应用的理想之选。

在电源启动期间或出现环境变化时，可通过内置逻辑电路自动执行校准功能。而且，由于配置了参数的初始设置，如增益，在应用推荐的开关模式时，LC717A00AR可单独工作。

此外，由于LC717A00AR的串行接口兼容I^2C和SPI总线，必要时可使用外部器件调整参数。此外，还可检测8输入电容数据输出并将其作为8位数据测量。

产品特性

- 检测系统：差分电容检测(互电容型)
- 输入电容分辨率：能检测到低至毫微微法拉的电容变化
- 测量间隔(8个差分输入)：
  - 18 ms (典型值) (初始配置)
  - 3 ms (典型值) (最小间隔配置)
- 外部测量元件：不需要
- 电流消耗：
  - 320 mA (典型值) (V_{DD} = 2.8 V)
  - 740 mA (典型值) (V_{DD} = 5.5 V)
- 电源电压：2.6 V至5.5 V
- 检测操作：开关
- 封装：VCT28
- 接口：可选择兼容I^2C * 的总线或SPI。

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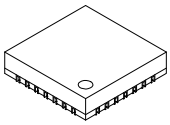


VCT28
CASE 601AE

MARKING DIAGRAM

XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

规格

Table 1. ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	V_{DD}	−0.3 to +6.5	V	
Input Voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V	(Note 1)
Output Voltage	V_{OUT}	−0.3 to V_{DD} + 0.3	V	(Note 2)
Power Dissipation	$P_{d\ max}$	160	mW	T_A = +105°C, Mounted on a substrate (Note 3)
Peak Output Current	I_{OP}	±8	mA	Per terminal, 50% Duty ratio (Note 2)
Total Output Current	I_{OA}	±40	mA	Output total value of LSI, 25% Duty ratio
Storage Temperature	T_{stg}	−55 to +125	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
(参考譯文)
如果电压超过最大额定值表中列出的值范围，器件可能会损坏。如果超过任何这些限值，将无法保证器件功能，可能会导致器件损坏，影响可靠性。

1. Apply to Cin0 to 7, Cref, nRST, SCL, SDA, SA, SCK, SI, nCS, GAIN.
2. Apply to Cdrv, Pout0 to 7, SDA, SO, ERROR, INTOUT.
3. 4-layer glass epoxy board (40 × 50 × 0.8t mm).

Table 2. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Remarks
Operating Supply Voltage	V_{DD}		2.6	−	5.5	V	
Supply Ripple + Noise	V_{PP}		−	−	±20	mV	(Note 4)
Operating Temperature	T_{opr}		−40	25	105	°C	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
推薦的工作範圍：
高于推荐工作范围表格中所列电压时，不保证能够正常运行。长时间在推荐工作范围表格中规定范围以外的电压下运行，可能会影响器件的可靠性。

4. Inserting a high-valued capacitor and a low-valued capacitor in parallel between V_{DD} and V_{SS} is recommended. In this case, the small-valued capacitor should be at least 0.1 μF, and is mounted near the LSI.

Table 3. ELECTRICAL CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 2.6 to 5.5 V, T_A = −40 to +105°C, Unless otherwise specified, the Cdrv drive frequency is f_{CDRV} = 143 kHz. Not tested at low temperature before shipment.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Remarks
Capacitance Detection Resolution	N		−	−	8	bit	
Output Noise RMS	N_{RMS}	Minimum gain setting	−	−	±1.0	LSB	(Notes 5, 7)
Input Offset Capacitance Adjustment Range	$Coff_{RANGE}$		−	±8.0	−	pF	(Notes 5, 7)
Input Offset Capacitance Adjustment Resolution	$Coff_{RESO}$		−	8	−	bit	
Cin Offset Drift	Cin_{DRIFT}	Minimum gain setting	−	−	±8	LSB	(Note 5)
Cin Detection Sensitivity	Cin_{SENSE}	Minimum gain setting	0.04	−	0.12	LSB/fF	(Note 6)
Cin Pin Leak Current	I_{Cin}	Cin = Hi−Z	−	±25	±500	nA	
Cin Allowable Parasitic Input Capacitance	Cin_{SUB}	Cin against V_{SS}	−	−	30	pF	(Notes 5, 7)
Cdrv Drive Frequency	f_{CDRV}		100	143	186	kHz	
Cdrv Pin Leak Current	I_{CDRV}	Cdrv = Hi−Z	−	±25	±500	nA	
nRST Minimum Pulse Width	t_{NRST}		1	−	−	μs	(Note 5)
Power-on Reset Time	t_{POR}		−	−	20	ms	(Note 5)

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{SS} = 0 V, V_{DD} = 2.6 to 5.5 V, T_A = −40 to +105°C, Unless otherwise specified, the Cdrv drive frequency is f_{CDRV} = 143 kHz. Not tested at low temperature before shipment.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Remarks
Power-on Reset Operation Condition: Hold Time	t_{POROP}		10	−	−	ms	(Note 5)
Power-on Reset Operation Condition: Input Voltage	V_{POROP}		−	−	0.1	V	(Note 5)
Power-on Reset Operation Condition: Power Supply Rise Rate	t_{VDD}	0 V to V_{DD}	1	−	−	V/ms	(Note 5)
Pin Input Voltage	V_{IH}	High input	0.8 V_{DD}	−	−	V	(Notes 5, 8)
	V_{IL}	Low input	−	−	0.2 V_{DD}		
Pin Output Voltage	V_{OH}	High output (I_{OH} = +3 mA)	0.8 V_{DD}	−	−	V	(Note 9)
	V_{OL}	Low output (I_{OL} = −3 mA)	−	−	0.2 V_{DD}		
SDA Pin Leak Current	$V_{OL\ I^2C}$	SDA Low output (I_{OL} = −3 mA)	−	−	0.4	V	
Pin Leak Current	I_{LEAK}		−	−	±1	μA	(Note 10)
Current Consumption	I_{DD}	When stand-alone configuration and non-touch V_{DD} = 2.8 V	−	320	390	μA	(Notes 5, 7)
		When stand-alone configuration and non-touch V_{DD} = 5.5 V	−	740	900		
	I_{STBY}	During Sleep process	−	−	1	μA	(Note 7)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
(參考譯文)
除非另有说明，“电气特性”表格中列出的是所列测试条件下的产品性能参数。如果在不同条件下运行，产品性能可能与“电气特性”表格中所列性能参数不一致。

5. Design-guaranteed values (not tested before shipment).
6. Measurements conducted using the test mode in the LSI.
7. T_A = +25°C.
8. Apply to nRST, SCL, SDA, SA, SCK, SI, nCS, GAIN.
9. Apply to Cdrv, Pout0 to 7, SO, ERROR, INTOUT.
10. Apply to nRST, SCL, SDA, SA, SCK, SI, nCS, GAIN.

Table 4. I²C COMPATIBLE BUS TIMING CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 2.6 to 5.5 V, T_A = −40 to +105°C, Not tested at low temperature before shipment.)

Parameter	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit	Remarks
SCL Clock Frequency	f_{SCL}	SCL		−	−	400	kHz	
START Condition Hold Time	$t_{HD;STA}$	SCL, SDA		0.6	−	−	μs	
SCL Clock Low Period	t_{LOW}	SCL		1.3	−	−	μs	
SCL Clock High Period	t_{HIGH}	SCL		0.6	−	−	μs	
Repeated START Condition Setup Time	$t_{SU;STA}$	SCL, SDA		0.6	−	−	μs	(Note 11)
Data Hold Time	$t_{HD;DAT}$	SCL, SDA		0	−	0.9	μs	
Data Setup Time	$t_{SU;DAT}$	SCL, SDA		100	−	−	μs	(Note 11)
SDA, SCL Rise/Fall Time	t_r / t_f	SCL, SDA		−	−	300	μs	(Note 11)
STOP Condition Setup Time	$t_{SU;STO}$	SCL, SDA		0.6	−	−	μs	
STOP-to-START Bus Release Time	t_{BUF}	SCL, SDA		1.3	−	−	μs	(Note 11)

11. Design-guaranteed values (not tested before shipment).

Table 5. SPI BUS TIMING CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 2.6 to 5.5 V, T_A = −40 to +105°C, Not tested at low temperature before shipment.)

Parameter	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit	Remarks
SCK Clock Frequency	f_{SCK}	SCK		−	−	5	MHz	
SCK Clock Low Time	t_{LOW}	SCK		90	−	−	ns	(Note 12)
SCK Clock High Time	t_{HIGH}	SCK		90	−	−	ns	(Note 12)
Input Signal Rise/Fall Time	t_r / t_f	nCS, SCK, SI		−	−	300	ns	(Note 12)
nCS Setup Time	$t_{SU;NCS}$	nCS, SCK		90	−	−	ns	(Note 12)
SCK Clock Setup Time	$t_{SU;SCK}$	nCS, SCK		90	−	−	ns	(Note 12)
Data Setup Time	$t_{SU;SI}$	SCK, SI		20	−	−	ns	(Note 12)
Data Hold Time	$t_{HD;SI}$	SCK, SI		30	−	−	ns	(Note 12)
nCS Hold Time	$t_{HD;NCS}$	nCS, SCK		90	−	−	ns	(Note 12)
SCK Clock Hold Time	$t_{HD;SCK}$	nCS, SCK		90	−	−	ns	(Note 12)
nCS Standby Pulse Width	t_{CPH}	nCS		90	−	−	ns	(Note 12)
Output High Impedance Time from nCS	t_{CHZ}	nCS, SO		−	−	80	ns	(Note 12)
Output Data Determination Time	t_v	SCK, SO		−	−	80	ns	(Note 12)
Output Data Hold Time	$t_{HD;SO}$	SCK, SO		0	−	−	ns	(Note 12)
Output Low Impedance Time from SCK Clock	t_{CLZ}	SCK, SO		0	−	−	ns	(Note 12)

12. Design-guaranteed values (not tested before shipment).

上电复位(POR)

电源开启后，LSI内的上电复位启用，且在特定上电复位时间t_{POR}之后释放其状态。上电复位工作条件：电源电压上升率t_{VDD}必须至少为1 V/ms。

由于INTOUT引脚在释放上电复位状态的同时从“高电平”变为“低电平”，因此可从外部验证t_{POR}。

在上电复位状态期间，Cin、Cref和Pout未知。

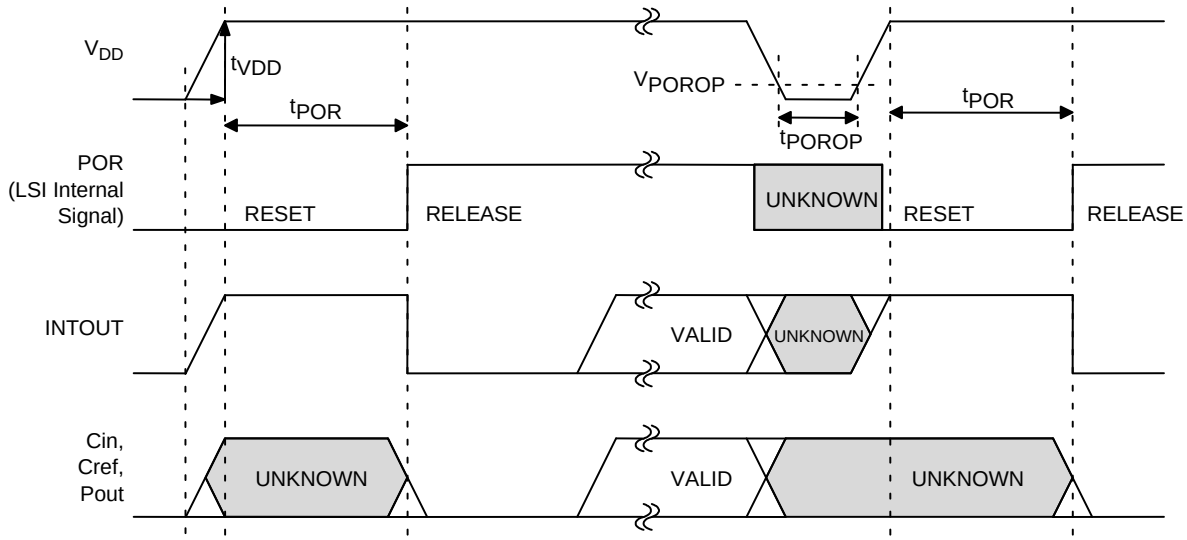


Figure 1.

I²C兼容总线数据计时

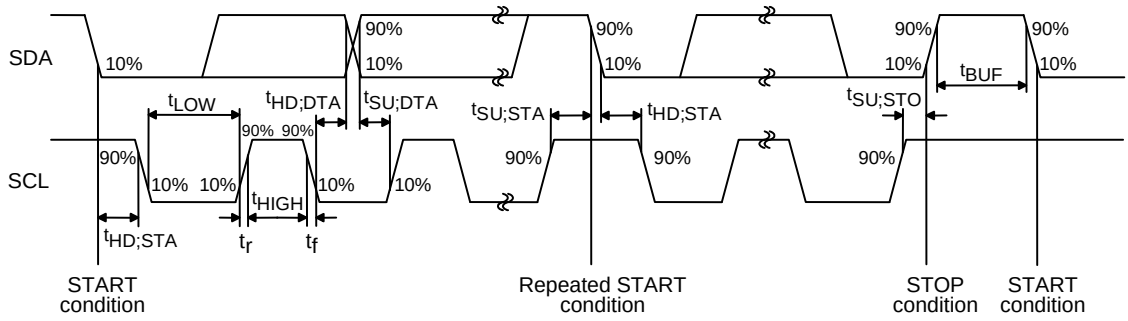


Figure 2.

I²C兼容总线通信格式

- 写入格式(可将数据写入按顺序递增的地址)

START	Slave Address	Write=L	ACK	Register Address (N)	ACK	Data written to Register Address (N)	ACK	Data written to Register Address (N+1)	ACK	STOP
			Slave		Slave		Slave		Slave	

Figure 3.

- 读取格式(可从按顺序递增的地址读取数据)

START	Slave Address	Write=L	ACK	Register Address (N)	ACK
			Slave		Slave

RESTART	Slave Address	Read=H	ACK	Data read from Register Address (N)	ACK	Data read from Register Address (N+1)	ACK	Data read from Register Address (N+2)	NACK	STOP
			Slave		Master		Master		Master	

Figure 4.

I²C兼容总线从地址

可通过SA端子选择两种地址。

Table 6.

SA Pin Input	7-bit Slave Address	Binary Notation	8-bit Slave Address
Low	0x16	00101100b (Write)	0x2C
		00101101b (Read)	0x2D
High	0x17	00101110b (Write)	0x2E
		00101111b (Read)	0x2F

SPI数据计时(SPI模式 0 /模式 3)

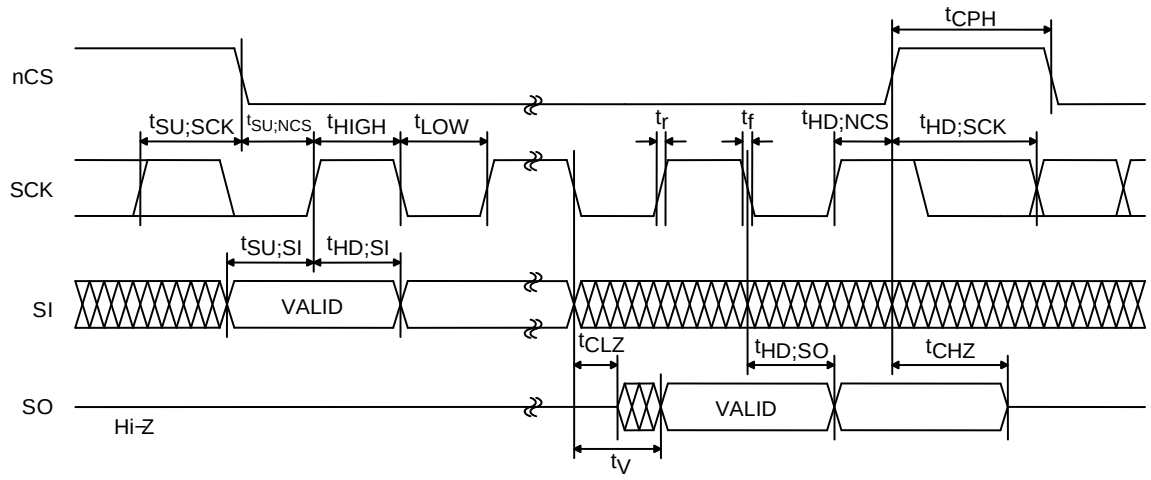


Figure 5.

SPI通信格式(模式 0示例)

- 写入格式(保持nCS = L时，可将数据写入按顺序递增的地址)

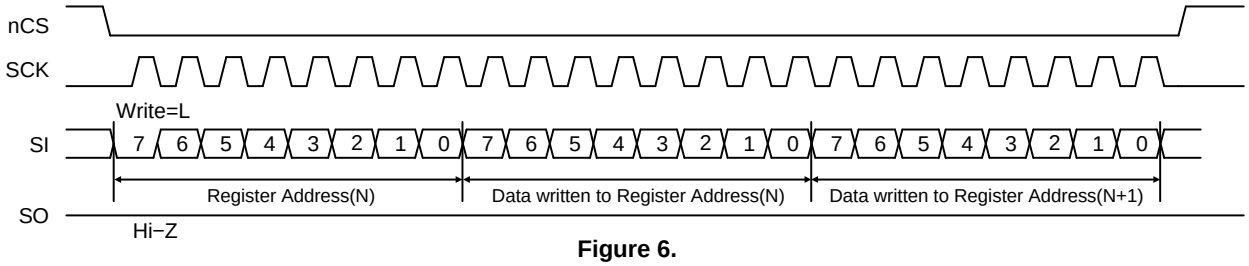


Figure 6.

- 读取格式(保持nCS = L时，可从按顺序递增的地址读取数据)

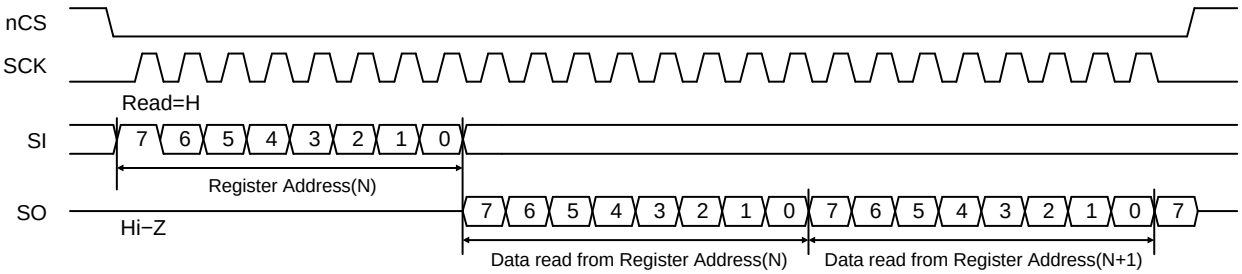


Figure 7.

框图

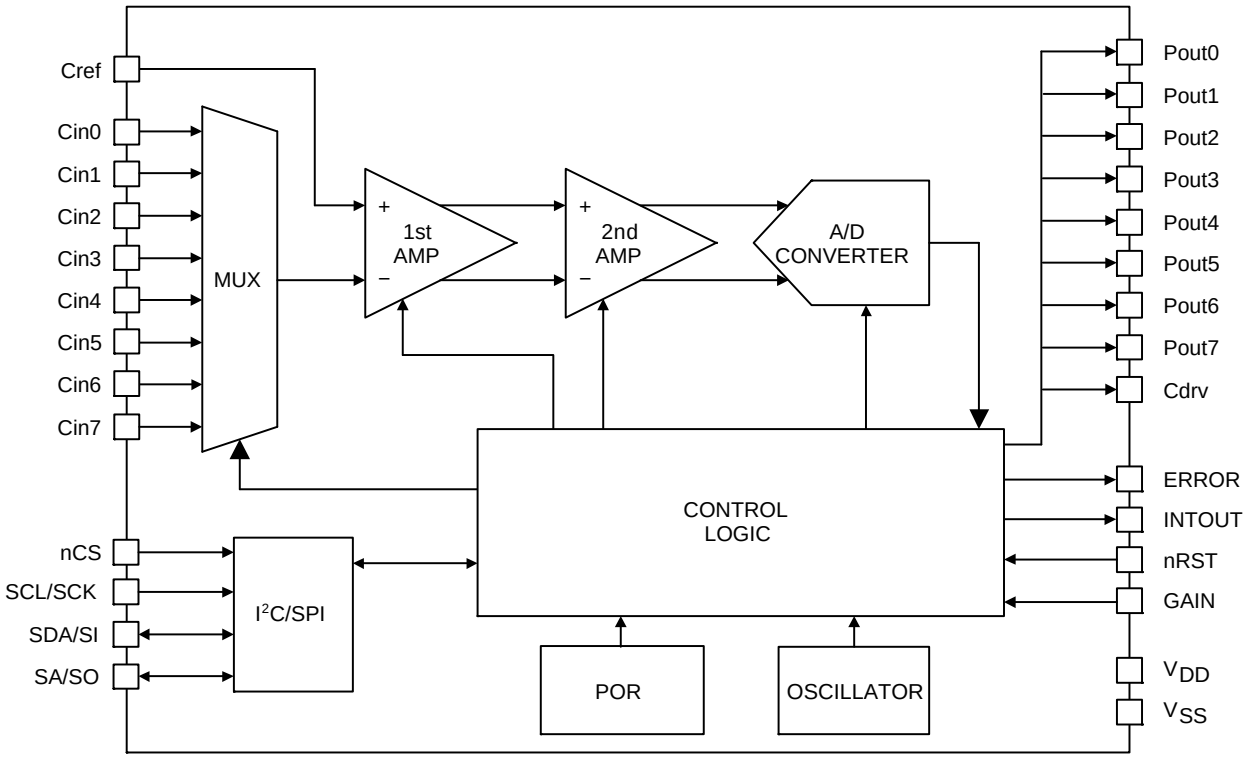


Figure 8. Block Diagram

LC717A00AR是一款电容数字转换器LSI，能低至毫微微法拉的电容变化。它由振荡电路(可产生系统时钟)、上电复位电路(电源开启后复位系统)、多工器(可选择输入通道)、两级放大器(可检测电容和输出模拟幅值变化)、A/D转换器(可将模拟幅值转换为数字数据)以及控制整个芯片的控制逻辑构成。此外，还带有I^2C兼容总线或SPI，必要时使用外部器件实现串行通信。

引脚分配

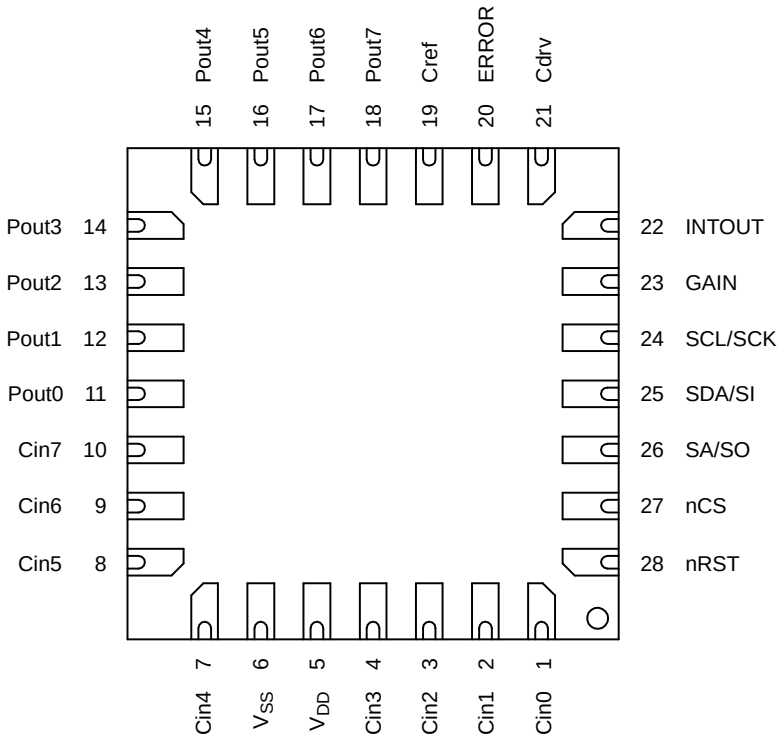


Figure 9. Pin Assignment

Table 7. PIN ASSIGNMENT

Pin No.	Pin Name	Pin No.	Pin Name
1	Cin0	15	Pout4
2	Cin1	16	Pout5
3	Cin2	17	Pout6
4	Cin3	18	Pout7
5	V_{DD}	19	Cref
6	V_{SS}	20	ERROR
7	Cin4	21	Cdrv
8	Cin5	22	INTOUT
9	Cin6	23	GAIN
10	Cin7	24	SCL/SCK
11	Pout0	25	SDA/SI
12	Pout1	26	SA/SO
13	Pout2	27	nCS
14	Pout3	28	nRST

Table 8. PIN FUNCTION

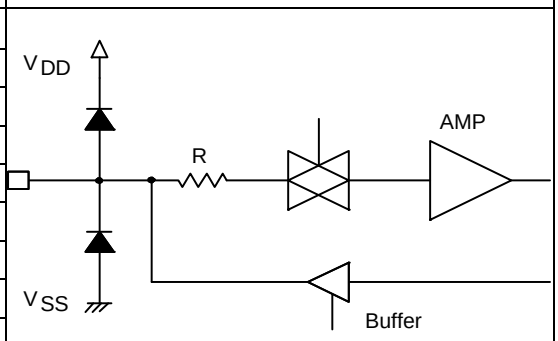
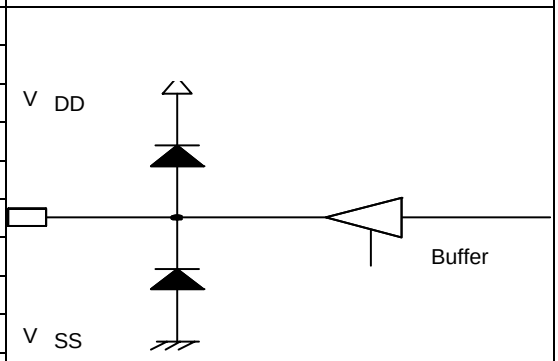
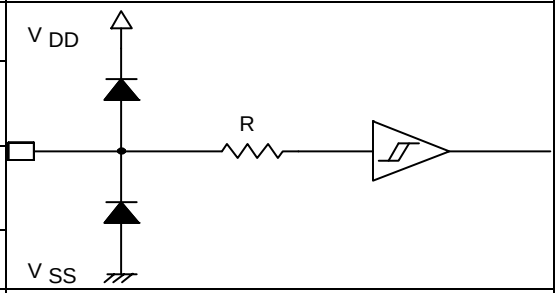
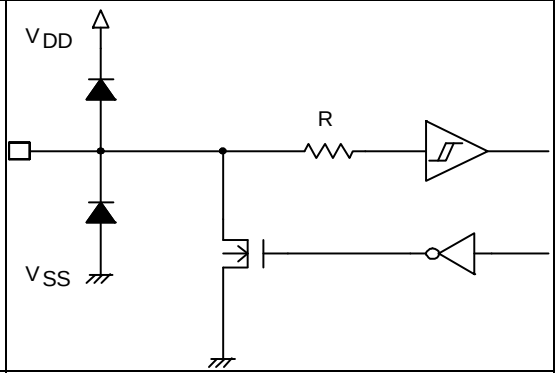
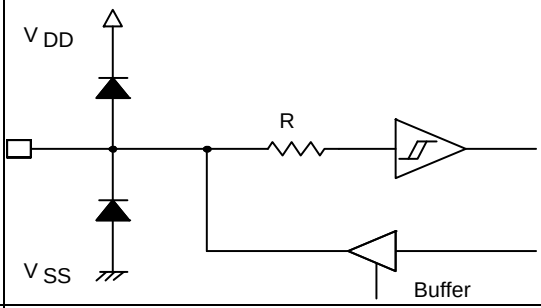
Pin Name	I/O	Pin Functions	Pin Type
Cin0	I/O	Capacitance sensor input	
Cin1	I/O	Capacitance sensor input	
Cin2	I/O	Capacitance sensor input	
Cin3	I/O	Capacitance sensor input	
Cin4	I/O	Capacitance sensor input	
Cin5	I/O	Capacitance sensor input	
Cin6	I/O	Capacitance sensor input	
Cin7	I/O	Capacitance sensor input	
Cref	I/O	Reference capacitance input	
Pout0	O	Cin0 judgment result output	
Pout1	O	Cin1 judgment result output	
Pout2	O	Cin2 judgment result output	
Pout3	O	Cin3 judgment result output	
Pout4	O	Cin4 judgment result output	
Pout5	O	Cin5 judgment result output	
Pout6	O	Cin6 judgment result output	
Pout7	O	Cin7 judgment result output	
ERROR	O	Error occurrence status output	
Cdrv	O	Output for capacitance sensors drive	
INTOUT	O	Interrupt output	
SCL/SCK	I	Clock input (I^2C) / Clock input (SPI)	
GAIN	I	Selection pin of the initial value of gain of the 2nd-amplifier	
nCS	I	Interface selection / Chip select inverting input (SPI)	
nRST	I	External reset signal inverting input	
SDA/SI	I/O	Data input and output (I^2C) / Data input (SPI)	

Table 8. PIN FUNCTION (continued)

Pin Name	I/O	Pin Functions	Pin Type
SA/SO	I/O	Slave address selection (I^2C) / Data output (SPI)	
V_{DD}		Power supply (2.6 V to 5.5 V) (Note 13)	
V_{SS}		Ground (Earth) (Notes 13, 14)	

13. Inserting a high-valued capacitor and a low-valued capacitor in parallel between V_{DD} and V_{SS} is recommended. In this case, the small-valued capacitor should be at least 0.1 μF, and is mounted near the LSI.
14. When V_{SS} terminal is not grounded in battery-powered mobile equipment, detection sensitivity may be degraded.

引脚功能详细信息

Cin0到Cin7

这些是电容传感器输入引脚。这些引脚用于连接至触摸开关模式。Cin和Cdrv的配线应彼此靠近。如此一来，Cdrv和Cin的配线将彼此电容耦合。因此，LSI可检测各配线附近的电容变化，作为8位数字数据。

然而，如果各配线的形状或Cdrv的电容耦合值不合适，可能无法正确检测电容变化。

在此LSI中，有一个两级放大器，可检测电容和输出模拟幅值的变化。Cin0到Cin7连接至LSI中第一放大器的反相输入。

测量期间，除了被测通道以外，其他通道均处于“低”状态。

将不使用的端子保持开路。

Cref

这是参考电容输入脚。此引脚的使用方法是：连接至Cin等引脚的配线使用此引脚，或连接此引脚和Cdrv引脚之间的任何电容。

在此LSI中，有一个两级放大器，可检测电容和输出模拟幅值的变化。Cref连接至LSI中第一放大器的非反相输入。

由于Cin引脚配线接头及配线中产生的寄生电容，以及Cin和Cdrv引脚配线间产生的寄生电容，Cref可能无法准确检测各Cin引脚的电容变化。在此情况下，可在Cref和Cdrv之间连接适当的电容，以准确检测电容变化。

然而，如果各Cin引脚寄生电容间的差异非常大，可能无法正确检测各Cin引脚的电容变化。

Pout0到Pout7

这些是检测结果输出引脚。Cin0到Cin7的电容检测结果将与LSI的阈值进行比较。引脚输出“高”还是“低”取决于该结果。

ERROR

这是错误发生状态输出引脚。在正常工作期间，将输出“低”。如果存在校准错误或系统错误，将输出“高”，以指示发生错误。

Cdrv

这是电容传感器驱动输出引脚。此引脚将输出在Cin0到Cin7检测电容所需的脉冲电压。

Cdrv和Cin配线应相互靠近，以便彼此电容耦合。

INTOUT

这是中断输出引脚。测量完成后，将输出“高”。如有必要，可连接至主微电脑，并用作中断信号。

如果不使用此端子，则要保持开路。

SCL/SCK

时钟输入(I^2C)/时钟输入(SPI)。这是I^2C兼容总线或SPI的时钟输入引脚，具体取决于工作模式。

如果不使用接口，则将引脚修正为“高”。然而，即使不使用接口，仍推荐在电路板上提供通信端子。

GAIN

在此LSI中，有一个两级放大器，可检测电容和输出模拟幅值的变化。这是第二放大器初始增益值的选择引脚。

即使单独使用此LSI，仍可通过此端子选择增益设置。初始化LSI时，若GAIN引脚为“低”，将设置为比最低设置高7倍，若GAIN引脚为“高”，则设置为比最低设置高14倍。

nCS

接口选择/芯片选择反相输入(SPI)。通过此端子选择I^2C兼容总线模式或SPI模式。初始化后，LSI自动进入I^2C兼容总线模式。若要继续使用I^2C兼容总线模式，将nCS引脚修正为“高”。若要在LSI初始化后切换至SPI模式，则将nCS输入从“高”更改为“低”。nCS引脚用作SPI的芯片选择反相输入引脚，将一直保持SPI模式，直到LSI再次初始化。

如果不使用接口，则将引脚修正为“高”。

nRST

这是外部复位信号反相输入引脚。当nRST引脚为“低”时，LSI进入复位状态。

在复位状态期间，各引脚(Cin0到7、Cref、Pout0至Pout7、ERROR)均为“Hi−Z”。

SDA/SI

数据输入和输出(I^2C)/数据输入(SPI)。这是I^2C兼容总线的数据输入和输出引脚，或SPI的数据输入引脚，具体取决于工作模式。

如果不使用接口，则将引脚修正为“高”。然而，即使不使用接口，仍推荐在电路板上提供通信端子。

SA/SO

从地址选择(I^2C)/数据输出(SPI)。这是I^2C兼容总线的从地址选择引脚，或SPI的数据输出引脚，具体取决于工作模式。

如果不使用接口，则将引脚修正为“高”。然而，即使不使用接口，仍推荐在电路板上提供通信端子。

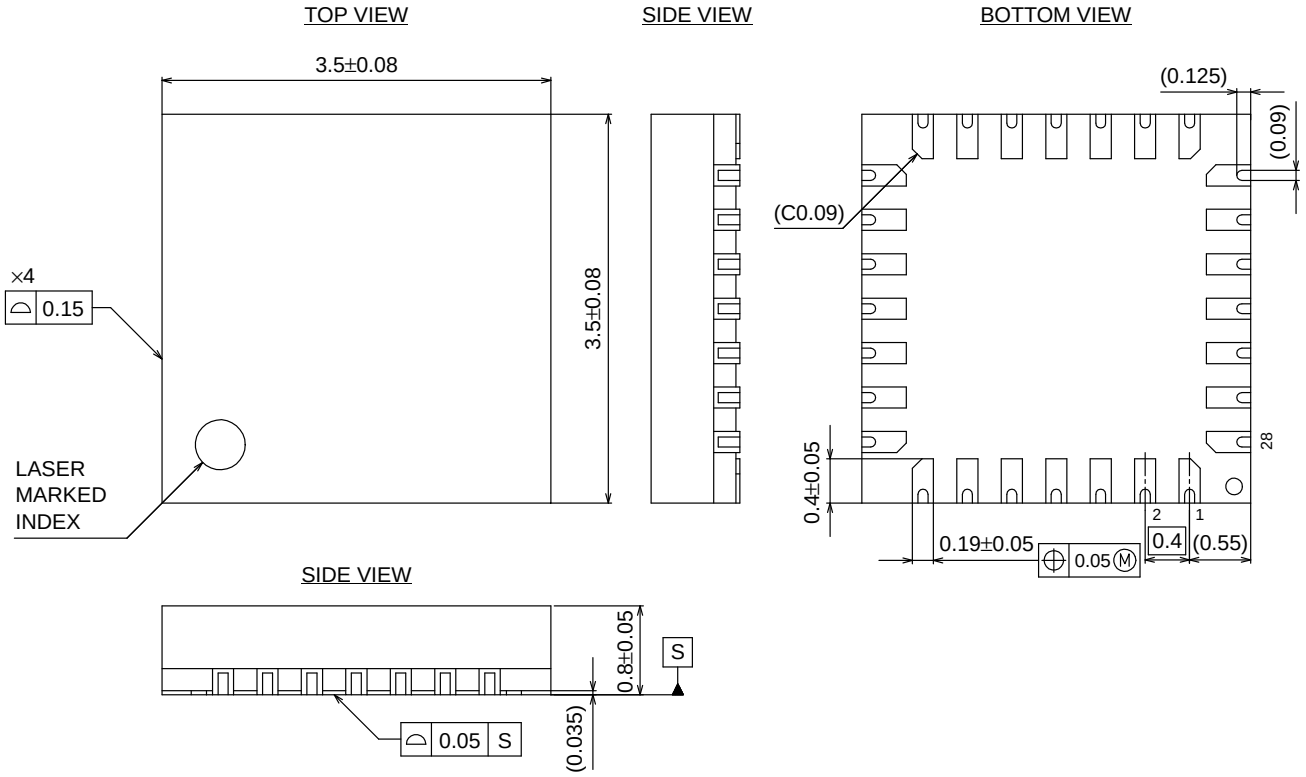
Table 9. ORDERING INFORMATION

Device	Package	Shipping†
TBD	VCT28 3.5 × 3.5 (Pb-Free)	TBD / Tape & Reel

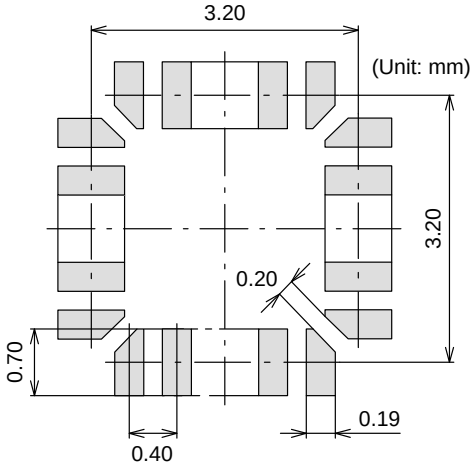
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

VCT28 3.5x3.5
CASE 601AE
ISSUE A



SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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