Accurate and Faster way to Silicon with EdXact

Ke Liu
Silvaco Overview

• Leading Electronic Design Automation (EDA) software and services provider founded in 1984
  • 400+ customers worldwide
  • 200+ employees with global footprint in United States, United Kingdom, France, Japan, Korea, China Taiwan, Singapore
  • Privately Owned - Financially strong and profitable
• Only provider delivering complete TCAD-to-Signoff product portfolio
  • TCAD, 3D RC extraction, SPICE modeling & simulation, Variation Analysis, Custom IC Design and Power Integrity Signoff
• Strong vertical solutions focus – Display, Power, Optical, Reliability, Advanced Process & Analog/Memory IP Development
• Silvaco adds advanced netlist reduction for SPICE simulation speed-up with acquisition of edXact
• Silvaco enters IP market with IPextreme acquisition
TCAD-to-Signoff

Custom Design
- Gateway Schematic Editor
- Expert Layout Editor
- Guardian DRC/LVS/NET
- Hipex Full Chip RCX

Variation Analysis
- Variation Manager
  - Fast MC
  - High Sigma
  - Library Verif

Power Integrity Signoff
- InVar
  - Power, IR
  - EM
  - Thermal

Netlist Reduction
- Jivaro

Characterization
- AccuCell
- AccuCore

SPICE Simulation
- SmartSpice
- SmartSpice RF
- SmartView
- Harmony AMS

Model Extraction
- Utmost IV Device Characterization and SPICE Modeling
- Spayn Statistical Analysis
- TechModeler Fast Modeling

3D RCX
- Clever RC Extractor
- Quest L Extractor
- Exact LPE File Generator

2D/3D TCAD
- Athena 2D Process
- Victory 3D Process
- Atlas 2D Device
- Victory 3D Device
- VWF DOE & Optimization

Block/IC Design & Verification

Process & Device Development
JIVARO

NETLIST REDUCTION ENGINES
Influence of Parasitics

- Parasitics on interconnections create unwanted behavior
  - Timing problems
  - Distortion
  - Cross-coupling
  - Noise on signals

- At 60nm RC delay (interco.) is more important than gate delay (unloaded delay)
Influence of Parasitics

• Simulation results are closer to reality
  • Better quality, time to market, time to volume

• On another hand the verification time databases increased

Impact of extracted RCC parasitics on transient simulation time for a 90nm design
The Burden of Parasitics

Postlayout: Simulation w/o parasitics
Postlayout: Adding parasitics

Parasitics degrade performance of all simulators
• Simulate an extracted netlist with parasitics can take a very long time

• Jivaro optimizes the extracted netlist for all simulators
  • By reducing the order of the parasitic matrices
  • Yields Less nodes, less components, smaller footprint
  • Allows a simulation with the same accuracy in a shorter time
• JIVARO in a few words
  • Independent parasitic reductor
    • All kinds of parasitics
    • Sits in between your extractor and simulator
  • Speed up your existing simulator
    • All kinds of Spice / Spice-like simulators
  • Reliable, powerful, innovative and flexible
JIVARO - Standalone flows

• Two different JIVARO exist, depending on the ASCII netlist format
  • JIVARO-A
    • SPICE (and SPICE like) and SPECTRE files with all R, C, L and K parasitics
    • openAccess databases (DM4 format) with all R, C, L and K parasitics
  • JIVARO-D
    • DSPF, SPEF and CalibreView files with all R, C, L and K parasitics
    • openAccess databases (DM4 format) with all R, C, L and K parasitics

• Possibility to use through
  • Graphical User Interface (GUI)
  • Command line
  • XML file
• A module of JIVARO allows the reduction directly from the Cadence Design System environment: **SALSA**

• **SALSA** has its own GUI and two different flows available
  • from an extracted view
  • from the Analog Design Environment (ADE L)

• Two others separated possibilities are available:
  • Reduction on the fly from a layout during the extraction
  • Reduction of an openAccess database

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openAccess database reduction flow will slowly replace the others integrated solutions
JIVARO - Tokens

• To reduce netlists: JIVARO-A or JIVARO-D
• To reduce an openAccess database: JIVARO-A or JIVARO-D with SALSA
• To reduce from extracted views, layout and ADE: JIVARO-A with SALSA
Reliability

• State of the art netlist reduction using Model Order Reduction approach

• Accuracy requirements are set by the user

• Mathematical controlled preservation of electrical characteristics
  • Input/output impedance / Pin to pin resistance and / or pin to pin delay

This allows Jivaro to be process-independent and versatile

<table>
<thead>
<tr>
<th></th>
<th>65nm</th>
<th>40nm</th>
<th>28nm</th>
<th>20nm</th>
<th>14nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reliable</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>
• Jivaro best performances
  • Starting from unreduced netlists
  • Complex and large parasitic structures
    • Include power NETs
    • RLCK
  • Simulations with high degree of accuracy
## Powerful

<table>
<thead>
<tr>
<th>Design</th>
<th>Reduction</th>
<th>Simulator family</th>
<th>Speedup</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Amplifier</td>
<td>95%</td>
<td>Spice / Spectre</td>
<td>71 x 1h11 -&gt; 1min.</td>
<td>&lt; 1% error</td>
</tr>
<tr>
<td>VCO</td>
<td>96%</td>
<td>Spice / Spectre</td>
<td>Impossible -&gt; 25min</td>
<td>&lt; 1% error</td>
</tr>
<tr>
<td>Divider</td>
<td>85%</td>
<td>Spice / Spectre</td>
<td>20 x 5min -&gt; 15s</td>
<td>Designer validated</td>
</tr>
<tr>
<td>Memory</td>
<td>96%</td>
<td>Fast Spice</td>
<td>Impossible -&gt; 6h</td>
<td>Designer validated</td>
</tr>
</tbody>
</table>

- Important gain in productivity and quality due to important gain in speed by keeping accuracy
Recent examples:

- 5 test cases (Mixed and digital) pre-reduced during extraction, spice engine
  - Overall simulation time with Spice: 72h50mn
  - Reduction time cumulated: 1h20mn, around 40% reduction rate
  - 49h simulation time with reduced netlists
  - 1h20mn of Jivaro saved 24h of simulation

- Memory characterization pre-reduced during extraction with fastSpice engine
  - Original simulation time: 160h
  - Reduction time: 50mn, around 50% reduction rate
  - 128h simulation time with reduced netlists
  - 50mn of Jivaro saved 2 days of simulation
JIVARO features several innovative methods

- Ability to merge multi finger devices
- Temperature aware reduction
- Selective reduction
• JIVARO allows more than M.O.R
• Selective reduction feature
• Apply different settings to different parts of the design

Innovative

- Apply standard reduction
- Apply very aggressive reduction
- Apply conservative reduction
- Apply specific reduction

- Critical Net
- Intermediate Net
- Non critical Net
- Power Net
Selective reduction example

<table>
<thead>
<tr>
<th>#netlist</th>
<th>Applied reduction</th>
<th>Decrease in parasitic impact on time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>none</td>
<td>n/a</td>
</tr>
<tr>
<td>2</td>
<td>conservative</td>
<td>/ 2.0</td>
</tr>
<tr>
<td>3</td>
<td>Selective (conservative on selected NETs, aggressive elsewhere)</td>
<td>/ 5.5</td>
</tr>
</tbody>
</table>
• Impact of merging multifinger devices

- Adding Jivaro: active reduction, critical 99%, others 95%
- Adding Jivaro: critical 99%, Others 95%
- Adding Jivaro: 99% accuracy
- Plus parasitics
- Post layout
- Schematic

Simulation runtime

Innovative
• Merge of multifinger devices example

<table>
<thead>
<tr>
<th>#netlist</th>
<th>Applied reduction</th>
<th>Decrease in parasitic impact on time</th>
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<tbody>
<tr>
<td>1</td>
<td>none</td>
<td>n/a</td>
</tr>
<tr>
<td>2</td>
<td>conservative</td>
<td>/ 15</td>
</tr>
<tr>
<td>3</td>
<td>Conservative + merge of parallel devices</td>
<td>/ 30</td>
</tr>
</tbody>
</table>
• Temperature aware reduction

- Jivaro reduces Rs and recompute TC1/TC2 parameters so that temperature behavior is similar
• Many flow integration methods
  • Inline binaries / GUI / Cadence interfaces

• Addresses all types of parasitics
  • R, RC, RCC, RLCK

• Supports all major netlist formats
  • Spice / Spectre / DSPF / SPF / SPEF / CalibreView

• Support of the openAccess database
• Your benefits with Jivaro
  • Speed up the parasitic analysis flow
  • Adapt the reduction to your objectives
    • Be secured when/where you want to favor accuracy preservation
    • Be aggressive when/where you want to favor simulation speed
  • Enable simulations even in toughest cases
  • Access to state of the art reduction solution
  • Have a single independant and adaptative solution for all cases

Reliable ✓  Powerful ✓  Innovative ✓  Flexible ✓
VISO

DESIGN ANALYSIS AND VERIFICATION
To compare, analyse and explore

- **ALPS**
  - Graphical Control Platform

- **Netlist files**

- **Viso**
  - Design Analysis and Verification

- **BELLEDONNE**
  - Layout comparison via extraction

- **BRENNER**
  - Netlist Matching

Parasitic view, Analysis results
1. Is this design worth simulating?

2. What are the most important contributors for parasitic Rs or delays?

3. How can I optimize my Power grid layout?

4. Is my power network well connected?

5. I need to evaluate/support/develop this new L.P.E flow

6. Is my parasitic extractor doing a good job?
To answer these questions Viso offers various analyses:

- Pin to pin equivalent R or RC Delay calculation
- NET to NET C reporting
- Detailed layer contribution to total R, RC Delay, NET to NET C
- Mesh (power or clock) analysis: IR drop, access resistance, RC delay distribution, EM
- DSPF cut NET and isolated pin detection
- Detection of dangling sections
- Overlay of GDSII on top of parasitic data
VISO’s strengths

- **Performance**
  - 10 mn to calculate 2 millions of pin to pin Res from a 8 GB RCC netlist, same accuracy as SPICE

- **Ease of use and flexibility**
  - GUI or command line
  - Various ways to select or exclude NETs or pins
  - No need to setup a SPICE bench
  - User friendly way to exploit the results in the GUI
A few snapshot

- Display of parasitics netlist with the layout overlayed
A few snapshot

- Display of parasitics netlist in 3D
• Pin to pin resistances

Each line in the GUI / row in the chart represents a pin to pin R / delay
Color code is influenced by value
• Pin to pin resistances

• Contribution from each layer can be given

For this pin to pin combination, poly1 represents 69.5 % of the total R

Note: contribution of each single resistance can be further detailed
A few snapshot

- Display of a power grid in 2D and 3D view - resistanceMap analysis
Conclusion

• Users of VISO
  • Broaden their physical design certification
  • Reduce physical design debug time
  • Reduce Power MOS physical design time
  • Save simulation resources
  • Build a more robust extraction flow
BELLEDONNE

COMPARISON OF EXTRACTED NETLISTS
To compare, analyse and explore

ALPS
Graphical Control Platform

Netlist files

BRENNER
Netlist Matching

BELLEDONNE
Layout comparison via extraction

viso
Design Analysis and Verification

Batch results, Graphs
What is the impact of these settings on parasitic extraction?

How can I report/demonstrate these changes to designers?

I need to evaluate / support this new L.P.E., how can I detect differences vs other tools?

We have this new version of the pdk, how does it compare to the previous one?

Should we include this L.P.E. option as part of our sign-off flow?
BELLEDONNE's Tools

• BELLEDONNE combines two capabilities
  • Calculation of parasitics related metrics
    • Number of pins / NETs / Rs / Cs... (=statistics)
    • pin to pin Rs
    • pin to pin Delays
    • NET to NET Cs

• Report of differences
  • Qualify and quantify the differences
  • Display the differences using the GUI
BELLEDONNE's Flow

• BELLEDONNE accepts different types of input
  • ASCII netlists:
    • DSPF
    • SPEF
    • CalibreView
  • Ability to perform cross formats comparison:
    • DSPF vs CalibreView
    • DSPF vs SPEF
    • SPEF vs CalibreView
BELLEDONNE's Strengths

- Performance
  - 2mn to compare over 2 millions of pin to pin Rs

- Ease of use and flexibility
  - GUI or command line
  - Easy and flexible way to define comparisons
  - No need to setup a SPICE bench
  - User friendly way to exploit the results in the GUI
BELLEDONNE Typical Flow

- **LPE #1 settings #1 / LPE #1 / PDK version #1 / no E.C.O. ...**
- **LPE #2 / PDK version #2 / no E.C.O. ...**

**A design**

- **netlist #1**
- **netlist #2**

**BRENNER™**
- Match Pins and Nets

**BELLEDONNE™**
- Compare
- Quantify and qualify differences
- Calculate pin to pin R & Delays
- Calculate NET to NET Cs

**Expected results ?**

- **YES**
  - Flow qualified !

- **NO**
  - **VISOTM**
    - Explore differences

Update
• Graphical user interface of a comparison result

A Few Snapshots

Plots for all (ref. values in X axis, comp. values in Y axis)
A Few Snapshots

• Graphical user interface of a comparison result

Plots for all (ref. values in X axis, comp. values in Y axis)
A few snapshots

- Alternative display result (histogram graph)
A few snapshots

• Points out of range
A few snapshots

- Information of the layer contribution

<table>
<thead>
<tr>
<th>Layer name</th>
<th>Value</th>
<th>% of total value</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2</td>
<td>12.5723</td>
<td>47.2769</td>
</tr>
<tr>
<td>M3</td>
<td>12.3776</td>
<td>46.5456</td>
</tr>
<tr>
<td>M2_INDDUM</td>
<td>0.592052</td>
<td>2.2263</td>
</tr>
<tr>
<td>M4</td>
<td>0.557177</td>
<td>2.06522</td>
</tr>
<tr>
<td>VIA3</td>
<td>0.257678</td>
<td>0.968975</td>
</tr>
<tr>
<td>ML</td>
<td>0.111251</td>
<td>0.421734</td>
</tr>
<tr>
<td>VIA2</td>
<td>0.110572</td>
<td>0.415797</td>
</tr>
<tr>
<td>VIA1</td>
<td>0.0131249</td>
<td>0.0493553</td>
</tr>
<tr>
<td>M3</td>
<td>0.857756</td>
<td>26.7214</td>
</tr>
<tr>
<td>M2</td>
<td>0.826109</td>
<td>25.7355</td>
</tr>
<tr>
<td>M2_INDDUM</td>
<td>0.592052</td>
<td>18.444</td>
</tr>
<tr>
<td>M4</td>
<td>0.517316</td>
<td>16.1158</td>
</tr>
<tr>
<td>VIA3</td>
<td>0.266892</td>
<td>8.31439</td>
</tr>
<tr>
<td>M1</td>
<td>0.0907293</td>
<td>2.82546</td>
</tr>
<tr>
<td>VIA2</td>
<td>0.0458989</td>
<td>1.42988</td>
</tr>
<tr>
<td>VIA1</td>
<td>0.013243</td>
<td>0.423554</td>
</tr>
</tbody>
</table>
A few snapshots

• Easy further exploration in VISO
A few snapshots

- Easy further exploration in VISO
Conclusion

• Users of BELLEDONNE
  • Build a more robust extraction flow
    • They evaluate the impact of various extraction parameters
    • Broaden set of information to their customers
  • Deliver quality in time
    • Extend coverage of tests
    • Go straight to the differences
  • Save simulation resources
    • By appropriately using BELLEDONNE as test engine

• Fast, accurate and easy comparison of different L.P.E. results
More than 20 design groups using edXact's tools. From RF to Digital through Analog, Mixed, Memory, ASICs
User Community

A number of our customers....