

ASIP Designer – Application-Specific Processor Design Made Easy

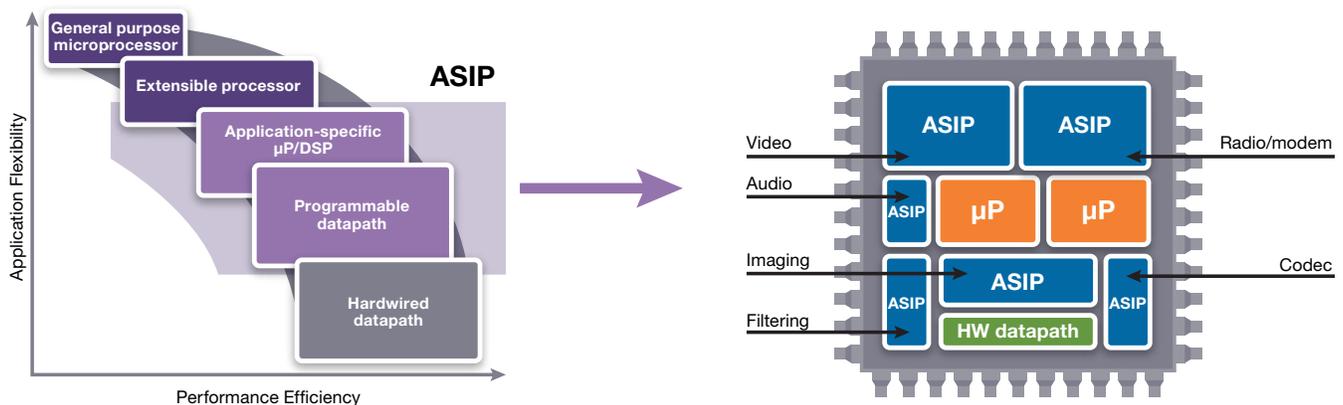


Figure 1: ASIP application flexibility and performance efficiency

Enabling the Design of Multicore SoCs with Application-Specific Instruction Set Processors

Offloading performance or power-critical functions from a merchant processor into specialized accelerators is commonplace in today's SoC designs. Such accelerators are specialized to the application in order to deliver the needed performance in the lowest power envelope, and they can be activated only when needed. These accelerators are implemented as application-specific instruction-set processors (ASIPs) or as fixed-function hardware.

The design of ASIPs comes with the need to define the best suited processor architecture, and to develop both the hardware implementation and the associated software development kit (SDK). So while the value of an ASIP is well-understood, SoC design teams have often gone back to standard processors because they were unable to complete an ASIP design on time and within budget.

Moving functions into hardware accelerators comes with a heavy cost, as well: loss of programmability, and therefore loss of flexibility after manufacture. This is intolerable with advanced process technology nodes, where high mask costs necessitate the reuse of silicon in multiple products and product generations, to expand the revenue lifetime of an SoC.

Fortunately, today's SoC designers can rely on tools such as Synopsys' ASIP Designer and MP Designer to build multicore SoCs with ASIPs. Such designs can be specialized to the application in order to meet the performance and power requirements, but still retain software programmability.

Automating application-specific instruction-set processor design – ASIP Designer

ASIPs rely on similar techniques as used in the design of hardware accelerators to reach high performance and low power: heavy use of parallelism and specialized datapath elements. Yet ASIPs retain software programmability within their application domain, resulting in C/C++ programmable processors and accelerators with the lowest power possible. ASIP Designer is a tool suite that brings ASIP design within easy reach of every SoC team. Key capabilities

include rapid exploration of architectural choices, generation of an efficient C/C++ compiler-based software development kit that automatically adapts to every architectural change, and automatic generation of power and area-optimized synthesizable RTL.

Bringing balance to multicore subsystems – MP Designer

SoC complexities are growing as more distinct system functions are combined in a single chip, requiring multicore architectures. Additionally, each system function (e.g. wireless modem, video coding, graphics) is becoming more complex, which may necessitate the introduction of multiple ASIPs for even a single system function. These evolutions bring new design challenges to system architects.

Notwithstanding the introduction of multicore subsystems, huge amounts of sequential, single-threaded application code are available and continue to be developed in the C language. Manually transforming such C code into parallel multithreaded software for a multicore subsystem is error-prone and requires costly and time-consuming verification. Furthermore, the multicore subsystem's performance will depend on the capabilities of the communication fabric between the different processor cores.

MP Designer is a tool suite that addresses these multicore subsystem design challenges. MP Designer supports C code parallelization for multicore subsystems, aiming at an efficient load-balancing and a low communication cost between the processor cores, while ensuring correct communication and synchronization between tasks running on different cores. MP Designer can also generate an efficient communication fabric.

Join our growing customer base

If offload, acceleration, flexibility, power optimization, and time-to-market are important to you, ASIP Designer and MP Designer may be just what you are looking for. Join the many semiconductor, system and IP companies that are shipping products today built with our tools. Proven applications areas include: wireless, wireline, vision, video, imaging, audio, wearable medical, security, automotive, industrial, network processing and high-performance computing. A wide range of example ASIP designs with highly

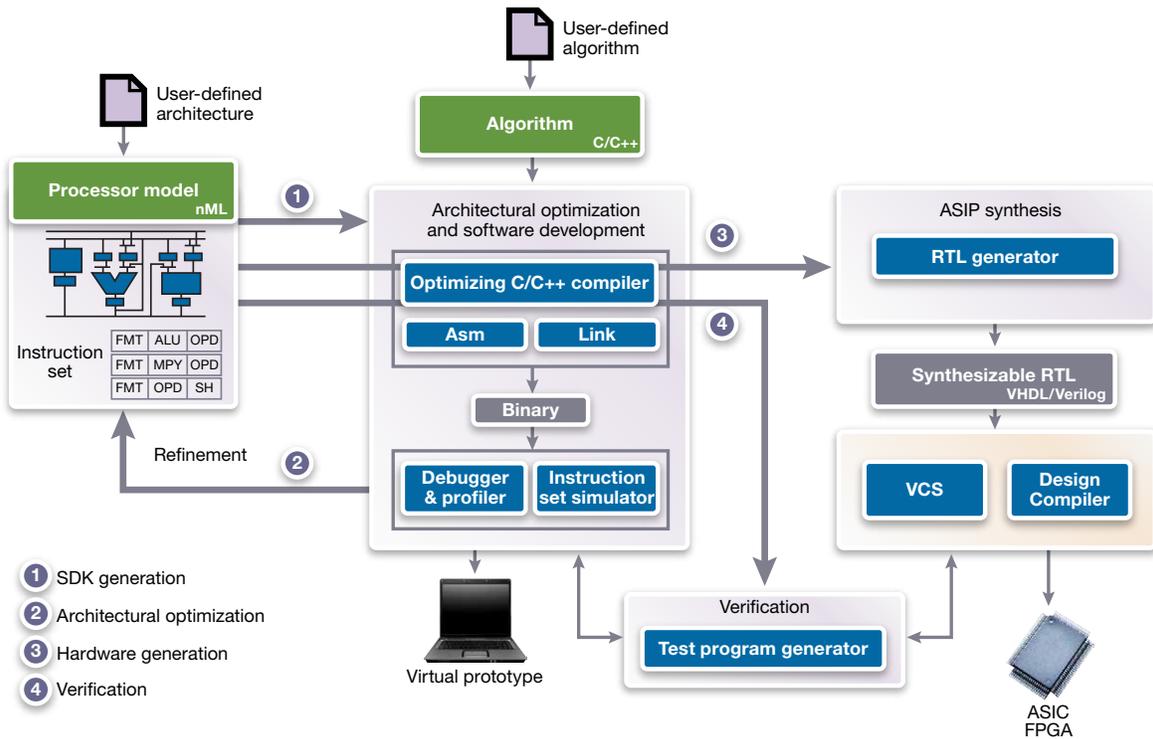


Figure 2: ASIP Designer tool suite

differentiating architectures provided in source code allows designers to quickly start designing their own ASIP targeting their specific application requirements.

Synopsys also offers modeling services relating to its ASIP Designer and MP Designer tool suites, to help its customers get to the market in the fastest possible way.

ASIP Designer

Architectural Exploration, Software Development Kit and Hardware Generation for ASIPs

ASIP Designer's patented technology supports the following features:

- ▶ Modeling of ASIP instruction-set architectures in the nML processor description language. Next to nML, the ASIP's periphery can be modeled in cycle- and bit-accurate C code. nML offers unprecedented architectural breadth enabling IP development for almost any vertical market.
- ▶ Unique compiler-in-the-loop technology, enabled by the automatic generation of a comprehensive software development kit (SDK) for each ASIP modeled in nML, containing the following components:
 - An optimizing compiler, recognized for its efficient code generation and quick and automatic retargetability to new ASIP architectures. The compiler supports ISO C99 (optionally extended with user-defined data types and operators using C++ classes and function overloading), C++, and OpenCL C

(OpenCL kernel language).

- A fast instruction-set simulator, offering both cycle-accurate and instruction-accurate abstraction levels and easy integration into signal-level and transaction-level (TLM2) virtual prototypes.
 - A flexible (multicore) debugger that can be used in connection to both instruction-set simulators and on-chip debug hardware (via JTAG).
 - Multi-faceted profiling capabilities to analyze the instruction-set architecture for hot-spots and to drive the architectural optimization process.
- ▶ Automatic generation of a power- and area-efficient hardware implementation of each ASIP, in synthesizable Verilog or VHDL.
 - ▶ Multi-faceted verification capabilities, including the automatic generation of ASIP-specific test programs in C and assembly code.

ASIP Programmer

Deployment of Software Development Kits to User Communities

Under Synopsys' ASIP Programmer service, ASIP-specific versions of the SDK, including optimizing C compiler, instruction-set simulator and debugger, can be created from the ASIP Designer tool suite. Such an ASIP-specific SDK can then be distributed to the user community of the ASIP, to enable the development and implementation of application software. Your customers obtain a high-quality, fully-featured SDK on the first day of availability of your ASIP.

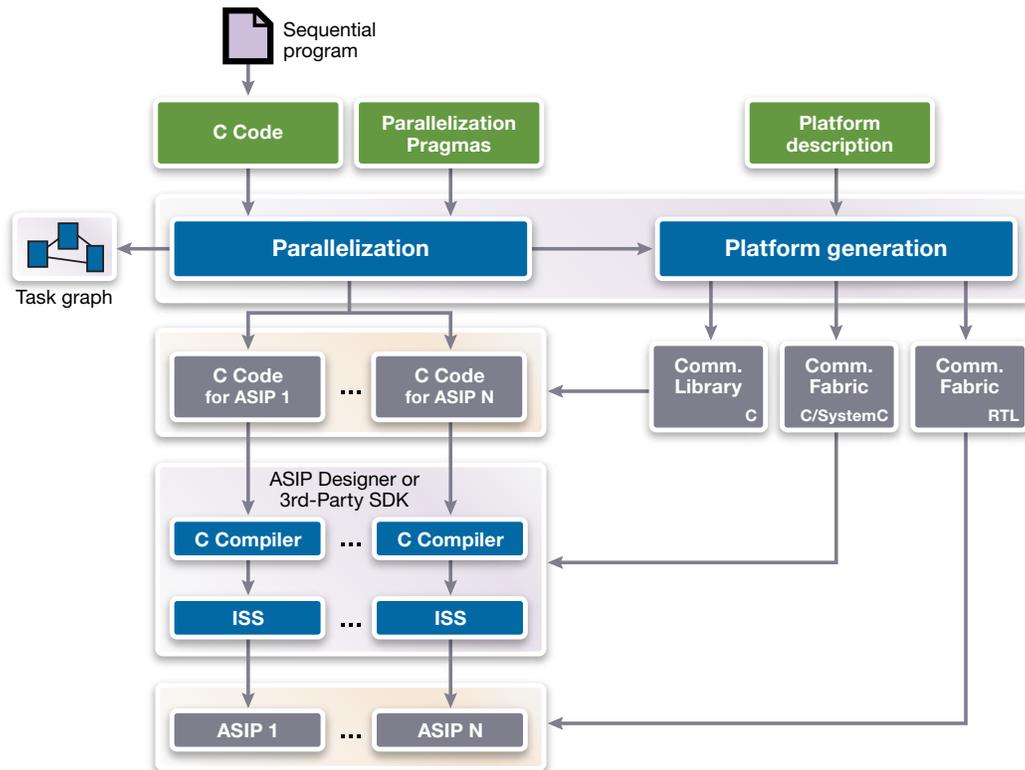


Figure 3: MP Designer tool suite

MP Designer

Software Parallelization and Platform Generation for Multicore SoCs

MP Designer's patented technology supports the following features:

- ▶ Homogeneous multicore architectures with shared memory, as well as heterogeneous architectures with point-to-point communication links using distributed memory.
- ▶ User-guided parallelization of sequential C source code, for implementation on multicore SoC architectures, exploiting both functional and data (loop-based) parallelization.
- ▶ Automatic global data-flow analysis of the code, to verify the feasibility of the parallelization proposed by the user.
- ▶ Automatic insertion of all required software code for communication and synchronization between tasks assigned to processors.
- ▶ Rapid feedback about performance, load balancing, memory and communication cost, visualized in the form of task graphs and temporal activity diagrams.
- ▶ Automatic generation of a low-latency, low-power communication fabric between the processor cores, generated as SystemC and RTL code.