MIPI IP Solutions

Highlights

- Complete single-vendor solution for mobile and mobile-influenced applications
- Proven MIPI CSI-2, DSI and I3C controllers
- Silicon-proven D-PHY and M-PHY
- Interoperable with multiple devices
- Power-optimized and compact design
- Synopsys' active participation and contribution in mobile ecosystem and MIPI Alliance enables advanced IP development
- Promoter member on the MIPI board of directors

Target Applications

- Automotive ADAS and infotainment
- Drones
- Digital cameras and image sensors
- IoT edge devices
- Augmented/virtual reality
- Multimedia SoC
- Mobile storage
- Displays

Overview

DesignWare® MIPI® IP solutions enable the interface between system-on-chips (SoCs), application processors, baseband processors and peripheral devices. Synopsys' broad portfolio of MIPI IP solutions consists of silicon-proven PHYs and controllers, verification IP, IP Prototyping Kits and Interface IP Subsystems.

As a promoter member on the MIPI board of directors and an active contributor to the MIPI Alliance working groups, Synopsys continues to support the ecosystem by developing high-quality, low-power, cost-effective, interoperable MIPI IP solutions that enable designers to deploy new features into their mobile, automotive and IoT devices. Utilizing a single-vendor solution allows designers to lower the risk and cost of integrating MIPI interfaces into SoCs and device ICs, while speeding time-to-market.

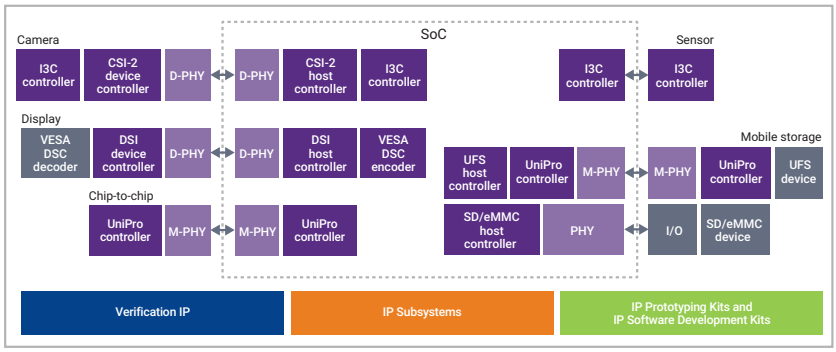

Figure 1: DesignWare MIPI IP solutions

DesignWare MIPI CSI-2 Controllers

Compliant with the MIPI CSI-2 specification, DesignWare MIPI CSI-2 Host and Device Controllers are fully-verified configurable IP solutions that provide a high-speed serial interface between an application or image processor and camera sensors. The controllers are architected to interface with the silicon-proven DesignWare MIPI D-PHY IP via the recommended PHY Protocol Interface (PPI), providing an easy to integrate and high-quality solution.

CSI-2 Features

- Compliant with the MIPI CSI-2 specification, v1.2
- PPI interface to D-PHY as recommended in the MIPI D-PHY specification, v1.2
- Configurable up to 8 data lanes at up to 2.5 Gbps per lane
- Supports all primary and secondary CSI-2 data formats
- Short and long packet formats
- Built-in test and debug capabilities
- Automatic generation of error correction code for the packet header, and checksum for the packet data
- Programmable multi-lane merging
- Detection of low-power and ultra low-power modes
- 64-bit pixel output format
- AMBA® APB control and configuration

DesignWare MIPI DSI Controllers

Compliant with the MIPI DSI specification, DesignWare® MIPI DSI Host and Device Controllers are fully-verified configurable IP solutions that provide a high-speed serial interface between an application processor and displays. The controllers are architected to interface with the silicon-proven DesignWare MIPI D-PHY IP via the recommended PHY Protocol Interface (PPI), providing an easy to integrate and high-quality solution.

DSI Features

- Compliant with the MIPI DSI Specification v1.2
- Supports dual MIPI DSI use case with VESA Display Stream Compression (DSC) v1.1 specifications
- Supports MIPI specifications:
  - Display Pixel Interface (DPI-2) v2.00
  - Display Bus Interface (DBI-2) v2.00
  - Display Command Set (DCS) v1.3
  - Stereoscopic Display Formats (SDF) v1.0
- Support video and command modes
- Supports dual MIPI DSI use case with VESA Display Stream Compression (DSC) v1.1 standard
- Configurable from 1 to 4 data lanes up to 2.5 Gbps per lane
- PPI interface to the D-PHY, as recommended in the MIPI D-PHY specification, v1.2
- Bidirectional communication and escape mode support
- Programmable display resolutions up to quad HD, 4K or higher
- Optimizes buffer size between MIPI DSI Host Controller and DSC encoder
- Supports 24-bit and 30-bit RGB video pixel formats
- ECC and checksum capabilities
- Supports ultra low-power mode
- Multiple peripheral support capability with configurable virtual channels

DesignWare I3C Controller

Synopsys' DesignWare MIPI I3C Controller IP is compliant with the latest I3C specification and delivers high bandwidth and scalability for integration of multiple sensors into mobile, automotive and IoT SoCs. The support for in-band interrupts within the 2-wire interface provides significantly lower pin count, simplifying board design and reducing power and cost. The IP is backward compatible with I^2C, allowing designers to future proof their design, and the master and slave operating modes enable systems with several ICs to efficiently connect to all sensors on a single I3C bus.

I3C Features

- Compliant with the latest MIPI I3C specification
- Backward compatible with the I^2C slave devices
- Supports all data rates up to 33.4 Mbps
- Supports master, secondary master and slave roles
- Supports in-band interrupts within the 2-wire interface
- Dynamic address allocation
- Hot-join capability
- Synchronous/asynchronous time control support
- Low-power management support
- 32-bit AMBA APB slave interface to application processor
- Optional simple register access interface
- Configurable external SRAM access
- Peripheral flow control mode in DMA handshaking interface support
- Fully interoperable with third-party I3C master and slave solutions

DesignWare MIPI D-PHY

The demand for enhanced multimedia features are pushing device manufacturers to integrate more advanced peripherals such as multi-megapixel cameras and larger screens into their designs. Integrating these capabilities into mobile devices brings new challenges to the industry in terms of power, performance, time-to-market and overall system costs. To address these challenges, the MIPI Alliance defines and promotes open interface specifications such as the Camera Serial Interface (CSI-2), Display Serial Interface (DSI), which all use the MIPI D-PHY specification. Synopsys offers a high-quality, low-power, silicon-proven D-PHY solution that is available today in a variety of advanced processes.

D-PHY Features

- Compliant with the MIPI D-PHY specification, v1.2
- Fully verified hard macro
- Up to 2.5 Gbps per lane
- Aggregate throughput up to 10 Gbps in 4 data lanes
- Support for the PHY Protocol Interface (PPI)
- Low-power escape modes and ultra low-power modes
- Shutdown mode
- SCAN and Loopback BIST modes
- Extensive access to internal programmability registers

DesignWare MIPI M-PHY

The DesignWare® MIPI® M-PHY supports multiple gears and a broad range of high-speed interfaces for applications including the JEDEC Universal Flash Storage (UFS), the MIPI Low Latency Interface (LLI) and UniPro interfaces. By providing an application-oriented M-PHY IP that operates at multiple speeds and is interoperable with multiple protocols, Synopsys enables design teams to "future- proof" their designs, while reducing the risk and cost of integrating MIPI interfaces into baseband, application processors and mobile integrated circuits (ICs).

M-PHY Features

- Compliant with the MIPI M-PHY specification, v4.1
- Supported protocols: MIPI UniPro, LLI, JEDEC UFS
- Supports High-Speed Gear1, Gear2, Gear3 A/B, and Gear4 A/B modes
- Supports M-PHY Type-I
- Modular architecture allows multiple lane configuration
- Low-speed Pulse-width Modulation (PWM) Gear1 to Gear5 in Type-I LS implementation
- Low-power operation, small area and low latency
- Future-proof for upcoming protocol enhancements
- Supports advanced process technologies
- Easily integrates with the DesignWare MIPI UniPro and UFS Host controllers

DesignWare UFS Host Controller

The DesignWare® Universal Flash Storage (UFS) Host Controller IP is a standard based serial interface engine for implementing a JEDEC UFS interface in compliance with the JEDEC UFS, UFS Host Controller Interface (UFSHCI) standards as well as the UFS removable card v1.1 and Unified Memory Extension (UME) standards. The DesignWare UFS Host Controller IP is a high-performance interface that is primarily used in applications where data is stored on non-volatile mass storage memory devices. The UFS Host Controller IP integrates the UFS host controller application layer with a pre-configured DesignWare MIPI® UniPro protocol stack that is optimized for UFS host application.

UFS Features

- Compliant with the JEDEC UFS, UFSHCI v3.0 and UFS card v1.1 standards
- Enables data and privacy protection using Incline Encryption (AES-XTS)
- Delivered as UFS host application layer integrated with DesignWare MIPI UniPro Controller IP, v1.8
- Manages UFS protocol between host and external UFS device
- Supports M-PHY v4.1 and access to M-PHY attributes
- Supports multiple lanes in HS-Gear4
- Compliant with the Unified Memory Extension (UME) specification
- Low-power operation, small area, and low latency
- Power gating, use of UPF, and auto hibernate feature

DesignWare MIPI UniPro Controller

The Unified Protocol (UniPro) specification defines a layered protocol for interconnecting devices and components within mobile device systems. Applicable to a wide range of component types including application processors, co-processors, and modems, as well as different types of data traffic including control messages, bulk data transfer and packetized streaming. Implementing the UniPro specification reduces time-to-market and design costs by simplifying the interconnection of peripherals. In addition, the re-useable, extensible nature of the specification simplifies new feature implementation.

UniPro Features

- Compliant with the MIPI UniPro specification, v1.8
- Supports all host and device configurations for JEDEC UFS, and UniPort-M
- Supports HS-Gear4 DesignWare M-PHY IP v4.1 and access to attributes
- HS-Gear4 adaptation and advanced granularity capability
- Low-power operation, small area and low latency
- Supports clock and power gating using Unified Power Format (UPF)
- Skip symbol insertion, scrambler function, MK2 extension
- Scalable maximum bandwidth (up to 4 lanes in each direction)
- Configurable number of C Ports and DDB settings

IP Accelerated Initiative

The Synopsys IP Accelerated initiative augments Synopsys' established, broad portfolio of silicon-proven DesignWare IP with new DesignWare IP Prototyping Kits, DesignWare IP Virtual Development Kits, and customized IP subsystems to accelerate prototyping, software development, and integration of IP into SoCs.

For hardware engineers, the IP Prototyping Kits provide a validated IP configuration that can be easily modified to explore design tradeoffs for the target application. Software developers can use either the IP Virtual Development Kits or the IP Prototyping Kits as proven targets for early software development, bring-up, debug and test.

Verification IP

Verification IP (VIP) for MIPI is built upon SystemVerilog UVM-based architecture to provide superior ease-of-use, performance, testbench productivity, and debug to speed and simplify verification of the most complex SoC designs.

VIP for MIPI includes comprehensive test suites which are self-contained and design-proven testbenches. All test suites are delivered in SystemVerilog source code enabling users to easily customize or extend the environment to include unique application-specific tests or corner-case scenarios. Testbench development is accelerated with built-in verification plans, coverage bins, example tests and scenario libraries.

Deliverables for MIPI Controllers

- Databook
- Application notes
- Verilog RTL source code
- Synthesis scripts for Synopsys Design Compiler
- Verification testbenches and test configurations
- Sample software drivers (when applicable)
- Prototyping system available

Deliverables for MIPI PHYs

- Databook
- Application notes
- Integration guidelines
- Verilog behavioral model
- Abstract LEF and timing LIB files
- GDSII layout database
- Prototyping system available

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired interface IP, wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP Prototyping Kits, IP Virtualizer Development Kit and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit synopsys.com/designware.