DesignWare IP for Automotive Applications

Synopsys IP and prototyping solutions provide the fastest path from proof-of-concept to verified SoC for automotive applications. Synopsys DesignWare IP solutions are used to ensure high quality and reliability in applications from infotainment with vehicle connectivity, advanced driver assistance systems (ADAS) and mainstream microcontrollers (MCUs). In addition, DesignWare IP enables automotive SoC designers to implement the latest protocols required in new applications such as embedded vision, sensor fusion and cloud connectivity user interfaces. Synopsys’ stringent quality and reliability standards give automotive SoC designers confidence when developing their complex SoCs using the latest interface IP, processors, embedded memories and logic libraries in mainstream and advanced process nodes.

Advanced Driver Assistance Systems

ADAS is experiencing rapid adoption and growth in automotive systems enabled by advancements in the underlying driver assistance technology. Fueled by consumer interest and government regulations focused on improving road safety, auto makers are requiring semiconductor suppliers to implement new capabilities for pedestrian detection/avoidance, lane departure warnings and correction, traffic sign recognition, surround view, drowsiness monitor and others.
**Surround View**

Blind spot detection

**Park Assistance**

Traffic sign recognition

Emergency breaking

Pedestrian detection

Collision avoidance

Lane departure warning

Cross traffic alert

**Long-range radar**

**LIDAR**

**Camera**

**Short/medium range radar**

**Ultrasound**

**Figure 1. ADAS applications**

**Benefits of Synopsys DesignWare IP for ADAS**

- Industry’s widest selection of interface IP including LPDDR4, Ethernet AVB and TSN, MIPI, and HDMI offers high quality and reliability for driver assistance systems
- Vision processing IP supports the industry-leading Convolutional Neural Network (CNN) algorithm
- Sensor and Control IP Subsystem simplifies the addition of sensor fusion functions
- Security IP for cryptography and protocol acceleration offer platform security and secure boot

**Figure 2. IP for ADAS SoCs**

**Synopsys Solution for ISO 26262 Functional Safety**

- Synopsys “safety culture” implements policies, processes, strategies and safety managers (Semiconductor Automotive Functional Professional (SC-AFSP) certified) for safety-related IP development
- Enhanced safety features such as datapath protection, configuration register parity and ECC to memories
- IP delivered with ISO 26262 Safety Package
- Certified compliant by SGS-TUV Saar
- ASIL Ready IP include: Ethernet QoS, Embedded Memories, Embedded Test and Repair, ARC EM SEP and additional IP in progress or planned

**Infotainment**

Auto makers are planning the next-generation passenger experience to embrace the content explosion brought by smartphones and cloud connectivity. From embedded functions such as on-board navigation and satellite radio, to gesture recognition and Internet apps, infotainment growth is driving the need for flexible and adaptable solutions.

**Figure 3. Multimedia infotainment application**

**Benefits of Synopsys DesignWare IP for Infotainment**

- Support for multiple multimedia interfaces including proven Ethernet QoS IP designed to support real-time Audio Video Bridging and Timing Sensitive Networking (TSN)
- High-Performance Core (HPC) Design Kit with embedded memories and logic libraries ensures the highest performance for CPUs and DSPs
- Security IP for HDCP 2.2 and DTCP-IP increases content protection

**Figure 4. IP for infotainment SoCs**

**MCUs**

Typical new cars contain more than one hundred MCUs throughout the automotive platform. Engine control, body and chassis control, EV/HEV battery management, instrument clusters, on-board diagnostics and other applications continue to expand the requirements for automotive MCUs. In addition, the growth of non-optical and image sensors that monitor engine performance, stabilization, and climate control are driving the addition of sensor fusion capabilities to the MCUs.
Benefits of Synopsys DesignWare IP for MCU SoCs

- Industry’s broadest portfolio of interface IP, analog ADCs and DACs, high-performance datapath elements, embedded memories and logic libraries, and 32-bit ARC® processors and processor-based subsystems
- DesignWare Sensor and Control IP Subsystem optimized to process data from digital and analog sensors to offload host processors, enabling more power efficient processing of the sensor data
- ARC EM with Safety Enhancement Package (SEP) for ISO 26262 safety-compliant automotive applications

ARC EM with SEP includes error-correcting code (ECC), parity support, user-programmable watchdog timer and dual-core lockstep interface. It includes a ASIL D safety-certified compiler and extensive safety documentation to ease the ISO 26262 certification process.

Designed for Automotive Reliability

Synopsys DesignWare IP has been designed in accordance to Synopsys’ stringent automotive mission profile following automotive-specific design rules. Synopsys verifies physical IP with very high reliability automotive Parts Per Million (PPM) targets and critical specifications according to automotive Process Capability Index (Cpk) distributions.

Faster Time-to-Market

SoCs for ADAS, infotainment and MCUs are growing in complexity as they implement high-performance applications such as vision detection/correction as well as extensive multimedia content. To reduce the overall effort and cost of assembling and integrating IP into an SoC, Synopsys offers DesignWare Interface IP Subsystems. The subsystems consist of pre-validated, fully integrated solutions that utilize Synopsys’ IP and tools for the specific SoC application. In addition, DesignWare Interface IP Subsystems provide extra functionality and value over simply integrating a PHY and controller, e.g., common register interface between the PHY and controller, debug logic, and more. The Interface IP Subsystems include key protocols for automotive such as DDR, PCIe, USB, and Ethernet, as well as multiprotocol subsystems.

In addition to IP subsystems, Synopsys provides DesignWare IP Virtualizer Development Kits (IP VDK) which enable software engineers to start development months before the hardware design is complete, enabling full system bring-up to occur within days of silicon availability. The IP VDKs include a reference virtual prototype of a popular processor subsystem used in automotive SoCs. The IP VDKs provide a configurable model of the DesignWare IP as well as a Linux software stack and reference drivers.

The Synopsys HAPS family of FPGA-based prototyping solutions provides an integrated and scalable hardware/software solution enabling automotive SoC design and verification teams to improve their design schedules and avoid costly device re-spins.

DesignWare IP Prototyping Kits include a proven reference design of the target IP pre-loaded onto a HAPS-DX FPGA-based prototyping system and software development platform running Linux OS. The pre-verified IP configuration can easily be modified to explore design tradeoffs for various automotive applications.

Synopsys provides a comprehensive portfolio of high quality, silicon proven IP that enables designers to develop SoCs for applications such as ADAS. The DesignWare IP and system-level design solutions are optimized for high performance, low power and low latency, and support advanced process technologies from 28-nm to 16-nm/14-nm FinFET.
<table>
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<tr>
<th>DesignWare IP</th>
<th>Product Features for Automotive ADAS and Infotainment SoCs</th>
<th>Automotive ADAS SoCs Impact</th>
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<tr>
<td>LPDDR4 Controller and PHY</td>
<td>Low latency, multi-port memory controller and PHY supporting LPDDR4 SDRAM speeds up to 3200 Mbps.</td>
<td>Multi-port access to shared main memory enables protocol engines for embedded vision and high-performance heterogeneous processing.</td>
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<tr>
<td>Ethernet AVB/TSN Controller</td>
<td>10/100/1000 Ethernet supporting Audio Video Bridging and IEEE-1588 PTP with 1-step time stamping.</td>
<td>Independent traffic classes and bounded latency enables precisely synchronized real-time camera and sensor data.</td>
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<tr>
<td>MIPI D-PHY and Host Controllers for MIPI CSI-2 and DSI</td>
<td>2.5 Gbps per lane interface to image sensors and LCD displays contains flexible CSI-2 and DSI configurations.</td>
<td>Enables multiple interoperable camera and display scenarios to support widest range of SoC applications.</td>
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<td>HDMI</td>
<td>Combination HDMI and MHL Tx/Rx PHY and controller solutions supporting latest HDMI v2.0 with HDCP 2.2 support.</td>
<td>Ability to locate ADAS SoC remotely from video system as well as supporting MHL-based smartphone connectivity.</td>
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<td>Embedded Memories</td>
<td>HPC Design Kit optimized for SoC processors: CPU, GPU and DSP. Designed for demanding electro migration (EM) conditions. STAR Memory system with EEC support for multi-bit error correction.</td>
<td>Enables optimal implementation across all three dimensions: performance, power, and area. SEU mitigation enables highest reliability.</td>
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<td>Embedded Test and Repair</td>
<td>STAR Memory System integrated test, repair and diagnostic solution for embedded memories. STAR Hierarchical System for automated hierarchical test for all IP and logic blocks on an SoC.</td>
<td>Achieve low DPPM for designs needing up to ASIL D. Field algorithmic programability and mission mode testing improve reliability for functional safety applications.</td>
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<td>Sensor &amp; Control IP Subsystem</td>
<td>Optimized to process data from digital and analog sensors. Offload host processors to enable more power-efficient processing of the sensor data. Implemented using Synopsys’ 32-bit ARC EM processor with ASIL D ISO 26262 Functional Safety Package.</td>
<td>Reduces cost, complexity and development effort by pre-integrating sensor and actuator-specific IP blocks together with software in a single subsystem. Enables sensor fusion by consolidating multiple sensor inputs to the SoC.</td>
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<tr>
<td>EV Vision Processor</td>
<td>Multicore embedded vision architecture optimized for object detection implementing convolutional neural network (CNN) with OpenCV and OpenVX software programming environments.</td>
<td>Faster object detection for gaze detection and gesture recognition for in cabin vision applications in high productivity software environment.</td>
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<td>32-bit ARC Processor</td>
<td>ARC EM with Safety Enhancement Package (SEP) for ISO 26262 Functional Safety applications with integrated hardware safety features.</td>
<td>Optimized for low-power embedded automotive applications. Complete solution of IP, tools and documentation accelerate development of ASIL D certifiable systems.</td>
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<tr>
<td>Security IP</td>
<td>Broad array of content protection IP, hardware cryptographic engines and middleware, and embedded security modules with tRoot Secure Hardware Root of Trust identification and authentication.</td>
<td>Complete security IP portfolio helps prevent a wide range of evolving threats in connected cars such as theft, tampering, side channel attacks, malware and data breaches.</td>
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<td>USB Controller and PHY</td>
<td>Operates at USB 3.1/3.0/2.0 speeds, interoperable with all USB generations. Flexible configuration allows more memory for higher performance.</td>
<td>Enables infotainment SoCs to support next-generation user interfaces with 4K and higher resolution video, imaging, audio and social media applications.</td>
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<td>PCI Express Controller and PHY</td>
<td>PCIe 3.0 with embedded DMA supporting endpoint, root port or dual mode operation. Choose native or AMBA interfaces to support key automotive processors.</td>
<td>Popular chip-to-chip interface to add processor peripherals. Low power L1 sub-states provide lowest power operation.</td>
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<td>SATA 6G Host and Device Controller and PHY</td>
<td>Supports both SATA and eSATA including AHCI programming model support multiple ports, Command and FIS-based port multiplier. Integrated DMA and advanced power management.</td>
<td>SATA IP provides lower latency and higher bandwidth data transfers for HDDs and SSD storage. Advanced power management maximizes power savings.</td>
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<td>12-bit SAR ADC</td>
<td>High resolution up to 12-bit, 320MSPS ADC/DAC converters. High dynamic range and high speed for extended application range. Compatible with embedded flash.</td>
<td>Integrated ADC reduces system form factor and extends application range for fast moving signal processing for multimedia and ADAS.</td>
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<td>NVM</td>
<td>AEC Q100 Temperature Grade 0 qualified NVM replaces e-fuses for calibration and trimming applications. Few Time Programmable and Multi-Time Programmable EEPROM.</td>
<td>Ideal for sensors, power management, LCD controllers, and precision analog.</td>
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For more information on DesignWare IP for automotive applications, visit [www.synopsys.com/ip-automotive](http://www.synopsys.com/ip-automotive).