

EV6x Embedded Vision Processors with Safety Enhancement Package

Highlights

- Adds hardware safety features to EV6x vision processor with minimal area and power impact
- Supports ISO 26262 automotive safety standard
- Integrated Automotive Safety Integrity Level (ASIL) B, C, or D Ready hardware
- Supported by MetaWare EV Development Toolkit for Safety with ASIL D Ready compiler and graph mapping tool
- Extensive safety documentation eases certification process
- Available as an option for EV61, EV62, and EV64 processors

Target Applications

- Safety-critical automotive systems using AI and deep learning
- Self-driving cars
- Radar/lidar systems
- Advanced Driver Assistance Systems (ADAS)

Overview

The ASIL B, C, or D Ready DesignWare EV6x Embedded Vision Processors with Safety Enhancement Package (SEP) enable automotive system-on-chip (SoC) designers to accelerate Advanced Driver Assistance Systems (ADAS) and autonomous vehicle application development and ISO 26262 certification for systems using vision processing, artificial intelligence (AI) and deep learning. The EV6x with SEP includes state-of-the-art hardware safety features including diagnostic error injection, windowed watchdog timers, error classification, and software diagnostic tests as well as safety monitors and lockstep capabilities for safety-critical modules. These features enable designers to achieve high levels of fault coverage as required for ASIL certifications without a significant effect on performance, power or area compared to the non-ASIL Ready EV6x processor

The DesignWare EV6x Embedded Vision Processors are fully programmable and combine the flexibility of software solutions with the high performance and low power consumption of dedicated hardware. The EV6x family integrates up to four high-performance 32-bit scalar cores and 512-bit vector DSPs, and an optimized convolutional neural network (CNN) engine for fast and accurate object detection, classification and scene segmentation. For more information on the EV6x family, please visit synopsys.com/ev6x.

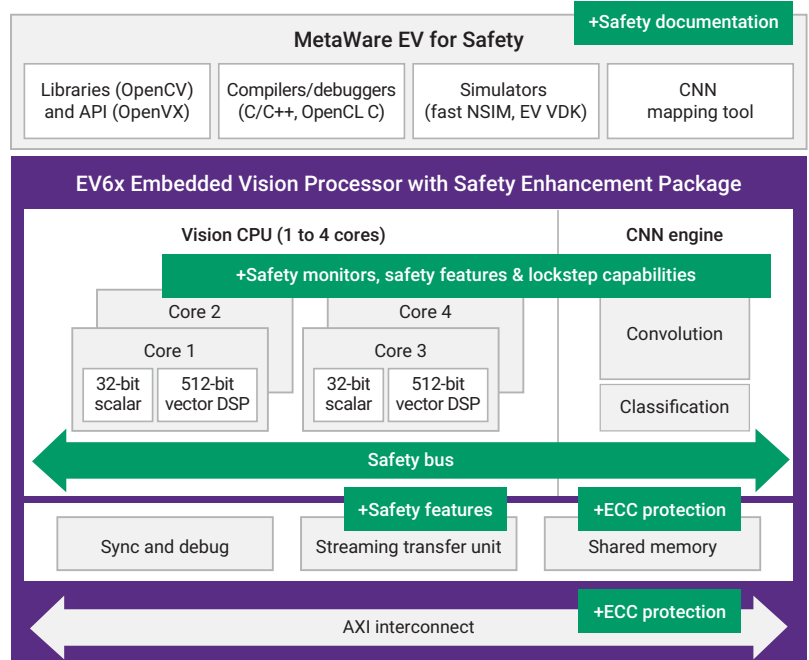


Figure 1: DesignWare EV6x Embedded Vision Processor with SEP

EV6x Processor Family Features

- Scalable from 1 to 4 vision CPU cores
- 32-bit scalar processing
- Wide vector DSP processing
- Up to 1.2GHz* performance with 10-stage pipeline
- Up to 8.6 TOPS* performance
- Optional Vector Floating Point Unit
- High-performance, programmable CNN engine, scalable from 880 to 1760 to 3520 MACs
- ARC® MetaWare EV Development Toolkit for Safety speeds software development for AI applications

EV6x with SEP Safety Features

- ASIL B, C, and D Ready options
- Integrated safety-critical hardware features
 - ECC memories
 - Diagnostic error injection
 - Error classification
 - Error checking on core registers and safety-critical registers
 - Windowed watchdog timer for each core
 - Software diagnostic tests
 - Lockstep capabilities for safety-critical modules
 - Optional dedicated Safety Island monitors and executes safety escalations and diagnostics within the SoC and protects system bring-up
- Safety documentation: FMEDA reports & safety manuals speeds functional safety assessments

ARC MetaWare EV Development Toolkit for Safety

To accelerate the development of ISO 26262-compliant code, Synopsys offers an ARC MetaWare EV Development Toolkit for Safety as a complete solution for developing, debugging, and optimizing embedded vision and AI applications for the EV6x processor with SEP. The toolkit supports development with C/C++ and OpenCL C programming languages and open standard environments, including OpenVX and OpenCV. A software development kit is also provided to map and optimize neural network graphs for the CNN engine. The compiler and graph mapping tools are ASIL D Ready to ease the certification process. The accompanying safety documentation helps developers of safety-critical systems to fulfill the requirements of the ISO 26262 standard. For more information on the ARC MetaWare EV Development Toolkit, visit synopsys.com/metaware.

| Component | Description |
|--------------------------------|------------------------------------------------------------------------------|
| MetaWare Compiler | Single ASIL D Ready compiler supports C/C++ & OpenCL C programming |
| MetaWare Debugger and nSIM | Debugger and simulator for debugging, profiling and optimizing |
| EV Runtime and Libraries | OpenVX and OpenVX SC frameworks and libraries eases vision graph development |
| CNN Software Development Kit | ASIL D Ready CNN graph mapping tools automates mapping to the CNN engine |
| EV Virtualizer Development Kit | System level simulation model with host for early development |

Table 1: MetaWare EV Development Toolkit For Safety components

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes [logic libraries](#), [embedded memories](#), [embedded test](#), [analog IP](#), [interface IP](#), [security IP](#), [embedded processors](#), and [subsystems](#). To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' [IP Accelerated initiative](#) offers [IP Prototyping Kits](#), IP software development kits, and [IP subsystems](#). Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit synopsys.com/designware.