DesignWare MIPI IP Solutions

Highlights

- Complete single-vendor solution for mobile and mobile-influenced applications
- Proven MIPI CSI-2, DSI and I3C controllers
- Silicon-proven D-PHY and M-PHY
- Interoperable with many devices in the market
- Enable power-optimized and compact design implementations
- Synopsys' active participation in mobile ecosystem and MIPI Alliance enables advanced IP development

Target Applications

- Applications processors
- Baseband processors
- Low-power SoC
- Image sensors
- Multimedia SoC
- Mobile storage
- Displays
- RFIC

Overview

DesignWare® MIPI® IP solutions enable the interface between system-on-chips (SoCs), application processors, baseband processors and peripheral devices. Synopsys' broad portfolio of MIPI IP solutions consists of silicon-proven PHYs and controllers, verification IP, IP Prototyping Kits and Interface IP Subsystems.

As a promoter member on the MIPI Board of Directors and an active contributor to the MIPI Alliance working groups, Synopsys continues to support the ecosystem by developing high-quality, low-power, cost-effective, interoperable MIPI IP solutions that enable designers to deploy new features into their mobile, automotive and IoT devices. Utilizing a single-vendor solution allows designers to lower the risk and cost of integrating MIPI interfaces into SoCs and device ICs, while speeding time-to-market.

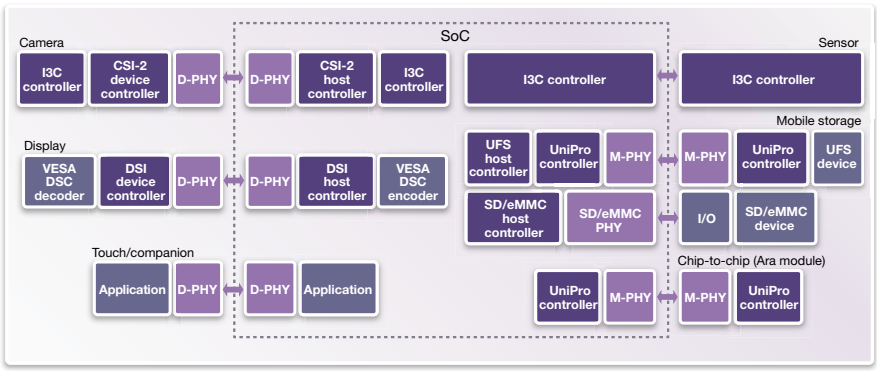

Figure 1. DesignWare MIPI IP solutions

CSI-2 Controllers

Compliant with the latest MIPI CSI-2 specification, DesignWare MIPI CSI-2 Host and Device Controllers are fully-verified configurable IP solutions that provide a high-speed serial interface between an application or image processor and camera sensors. The controllers are architected to interface with the silicon-proven DesignWare MIPI D-PHY IP via the recommended PHY Protocol Interface (PPI), providing an easy to integrate and high-quality solution.

Synopsys' DesignWare MIPI CSI-2 Host Controller IP, DesignWare MIPI CSI-2 Device Controller IP, DesignWare MIPI I3C Controller IP and DesignWare MIPI D-PHY IP provide a complete camera interface solution that enables designers to lower the risk and cost of integrating the MIPI CSI-2 IP into application processors, image signal processors and multimedia coprocessors, while improving the time-to-market demand of mobile, IoT and automotive SoCs.

CSI-2 Features

- Compliant with the MIPI CSI-2 specification, v1.2
- PPI interface to D-PHY as recommended in the MIPI D-PHY specification, v1.2
- Configurable up to 8 data lanes at up to 2.5 Gbps per lane
- Supports all primary and secondary CSI-2 data formats
- Short and long packet formats
- Built-in test and debug capabilities
- Automatic generation of error correction code for the packet header, and checksum for the packet data
- Programmable mlti-lane merging
- Detection of low-power and ultra low-power modes
- 64-bit pixel output format
- AMBA® APB control and configuration

DSI Controllers

Compliant with the latest MIPI DSI specification, DesignWare® MIPI DSI Host and Device Controllers are fully-verified configurable IP solutions that provide a high-speed serial interface between an application processor and displays. The controllers are architected to interface with the silicon-proven DesignWare MIPI D-PHY IP via the recommended PHY Protocol Interface (PPI), providing an easy to integrate and high-quality solution.

Synopsys' DesignWare MIPI DSI Host Controller IP, DesignWare MIPI DSI Device Controller IP and DesignWare MIPI D-PHY IP provide a complete display interface IP solution that enables designers to lower the risk and cost of integrating the MIPI DSI interface into application processors, display bridge ICs and multimedia coprocessors, while improving the time-to-market demand of mobile, IoT and automotive SoCs.

DSI Features

- Compliant with the MIPI DSI Specification v1.2
- Supports dual MIPI DSI use case with VESA Display Stream Compression (DSC) v1.1 standard
- Supports MIPI specifications:
  - Display Pixel Interface (DPI-2) v2.00
  - Display Bus Interface (DBI-2) v2.00
  - Display Command Set (DCS) v1.1
  - SDF v1.0
- Support video and command modes
- Supports dual MIPI DSI use case with VESA Display Stream Compression (DSC) v1.1 standard
- Configurable from 1 to 4 data lanes
- Supports up to 2.5 Gbps per data lane
- PPI interface to the D-PHY, as recommended in the MIPI D-PHY specification, v1.2
- Bidirectional communication and escape mode support
- Programmable display resolutions
- Video mode pixel formats: RGB565, RGB666 packed and loosely, RGB888
- ECC and checksum capabilities
- Supports ultra low-power mode

- Fault recovery schemes
- Multiple peripheral support capability with configurable virtual channels
- Integrated video pattern generator
- Supports transmission of all generic commands
- Configurable selection of system interfaces
- AMBA® APB control and configuration
- Packaged with Synopsys coreConsultant tool

I3C Controller

Synopsys' DesignWare MIPI I3C Controller IP is compliant with the latest I3C specification and delivers high bandwidth and scalability for integration of multiple sensors into mobile, automotive and IoT SoCs. The support for in-band interrupts within the 2-wire interface provides significantly lower pin count, simplifying board design and reducing power and cost. The IP is backward compatible with I2C, allowing designers to future proof their design, and the master and slave operating modes enable systems with several ICs to efficiently connect to all sensors on a single I3C bus. The standard-based ARM AMBA Advanced Peripheral Bus (APB) connects the IP to the rest of the SoC while the bus is connected to the register interface and the Direct memory Access (DMA) interface, offering easy IP integration. Low-power management features such as clock gating enable energy-efficient sensors and SoC designs while the configurable transaction and data buffering features enable performance versus cost tradeoffs for the target application.

I3C Features

- Packaged with Synopsys coreConsultant tool
- Compliant with the latest MIPI I3C specification
- Backward compatible with the I2C slave devices
- Supports all data rates up to 26.7 Mbps
- Supports in-band interrupts within the 2-wire interface
- Dynamic address allocation
- Hot-join capability
- Low-power management support
- 32-bit AMBA APB slave interface to application processor
- Configurable external SRAM access
- Peripheral flow control mode in DMA handshaking interface support
- Packaged with Synopsys coreConsultant tool

D-PHY

The demand for enhanced multimedia features are pushing device manufacturers to integrate more advanced peripherals such as multi-megapixel cameras and larger screens into their designs. Integrating these capabilities into mobile devices brings new challenges to the industry in terms of power, performance, time-to-market and overall system costs.

To address these challenges, the MIPI Alliance defines and promotes open interface specifications such as the Camera Serial Interface (CSI-2), Display Serial Interface (DSI), which all use the MIPI D-PHY specification.

D-PHY Features

- Compliant with the MIPI D-PHY specification, v1.2
- Fully verified hard macro
- Up to 2.5 Gbps per lane
- Aggregate throughput up to 10 Gbps in 4 data lanes
- Support for the PHY Protocol Interface (PPI)
- Low-power escape modes and ultra low-power modes
- Shutdown mode
- SCAN and Loopback BIST modess
- Extensive access to internal programmability registers
- Master, Slave, TX-only and RX-only configurations
- Attachable PLL for master applications
- Flexible input clock reference
- 50% DDR output clock duty cycle
- High-quality, silicon-proven design available on multiple process nodes and foundries

M-PHY

Synopsys' DesignWare® MIPI® M-PHY IP is compliant to the latest MIPI Alliance M-PHY specification and supports a wide range of high-speed interfaces for mobile applications including JEDEC Universal Flash Storage (UFS), USB SuperSpeed InterChip (SSIC), PCI-SIG M-PCIe™, MIPI UniPro, DigRF v4, Low Latency Interface (LLI) and future CSI-3 and DSI-2.

The DesignWare MIPI M-PHY IP supports High-Speed Gear1, Gear2 and Gear3 rates A/B along with Type-I and Type-II low-speed capabilities. The M-PHY's modular architecture allows implementation of a variety of transmitter and receiver lanes to meet a broad range of applications and all modes outlined in the protocol specification. A sophisticated clock recovery mechanism and power efficient clock circuitry are designed to guarantee the integrity of the clocks and signals required to meet strict timing requirements. The DesignWare MIPI M-PHY supports large and small amplitudes, slew rate control and dithering functionality for optimized electromagnetic interference (EMI) performance

M-PHY Features

- Compliant with the MIPI Alliance M-PHY specification, v3.1
- Supported protocols: MIPI UniPro, LLI, CSI-3, DSI, DigRF v4, JEDEC UFS, USB SuperSpeed Inter-chip (SSIC) and M-PCIe
- Supports High-Speed Gear1, Gear2 and Gear3 A/B modes
- Supports M-PHY Type-I and Type-II M-PORTs
- Modular architecture allows multiple lane configuration
- Low-Speed PWM Gears in Type-I LS implementation
- Low-power operation, small area and low latency
- Future-proof for upcoming protocol enhancements
- Supports advanced process technologies
- Easily integrated with the DesignWare MIPI UniPro or JEDEC UFS Host Controllers

UFS Host Controller

The DesignWare MIPI Universal Flash Storage (UFS) Host Controller IP is a standard based serial interface engine for implementing a JEDEC UFS interface in compliance with the JEDEC UFS, UFS Host Controller Interface (UFSHCI) standards as well as the UFS card v1.0 and Unified memory Extension (UME). The DesignWare MIPI UFS Host Controller is a high-performance interface that is primarily used in mobile devices where data is stored on non-volatile mass storage memory devices. The UFS Host Controller IP integrates the UFS host controller application layer with a pre-configured DesignWare MIPI UniPro protocol stack that is optimized for UFS host applications.

A standard-based synchronous bus system, such as OCP or AXI, connects the IP to the rest of the SoC. This bus is connected to the register interface and the DMA interface of the IP. The register and data structure implementation is based on the UFSHCI specification and is used by the UFS Host Controller's DMA engine. Leveraging industry standards in the UFS Host Controller ensures compatibility and performance.

UFS Features

- Compliant with the JEDEC UFS, UFSHCI v2.1 and UFS card v1.0 standards
- Enables data and privacy protection using Incline Encryption (AES-XTS
- Delivered as UFS host application layer integrated with DesignWare MIPI UniPro Controller IP, v1.61
- Manages UFS protocol between host and external UFS device
- Single traffic class
- Supports HS-Gear3 M-PHY v3.1 and ccess to attributes
- Supports multiple lanes in HS-Gear3
- Compliant with the UME specification
- Low-power operation, small area, and low latency
- Power gating, use of UPF flow and auto hibernate feature for power reduction

UniPro Controller

The Unified Protocol (UniPro) specification defines a layered protocol for interconnecting devices and components within mobile systems. Applicable to a wide range of component types including application processors, coprocessors, and modems, as well as different types of data traffic including control messages, bulk data transfer and packetized streaming. Implementing the UniPro specification reduces time-to-market and design costs by simplifying the interconnection of peripherals. In addition, the re-useable, extensible nature of the specification simplifies new feature implementation.

Synopsys' DesignWare MIPI UniPro Controller IP provides the capability to control the UniPro link over a multi-gear MIPI M-PHY link from one or more applications. Due to its generic nature, the MIPI UniPro Controller is capable of transporting any kind of data between applications like camera, display and memory devices on the same physical link.

UniPro Features

- Compliant with the MIPI UniPro specification, v1.61
- Supports all host and device configurations for JEDEC UFS, MIPI CSI-3, MIPI DSI and Google ARA UniPort-M
- Supports silicon-proven HS-Gear3 DesignWare M-PHY IP v3.1 and access to attributes
- Low-power operation, small area and low latency
- Supports power gating and use of Unified Power Format (UPF) flow
- HS-Gear3 adaptation and advanced granularity capability
- Skip symbol insertion, scrambler function, MK2 extension
- Scalable maximum bandwidth (up to 4 lanes in each direction)
- Configurable number of C Ports and DDB settings

Deliverables for MIPI Controllers

- Databook
- Application notes
- Verilog RTL source code
- Synthesis scripts for Synopsys Design Compiler
- Verification testbenches and test configurations
- Sample software drivers (when applicable)
- Prototyping system available

Deliverables for MIPI PHYs

- Databook
- Application notes
- Integration guidelines
- Verilog behavioral model
- Abstract LEF and timing LIB files
- GDSII layout database
- Prototyping system available

IP Accelerated Initiative

The Synopsys IP Accelerated initiative augments Synopsys' established, broad portfolio of silicon-proven DesignWare IP with new DesignWare IP Prototyping Kits, DesignWare IP Virtual Development Kits, and customized IP subsystems to accelerate prototyping, software development, and integration of IP into SoCs.

For hardware engineers, the IP Prototyping Kits provide a validated IP configuration that can be easily modified to explore design tradeoffs for the target application. Software developers can use either the IP Virtual Development Kits or the IP Prototyping Kits as proven targets for early software development, bring-up, debug and test.

Verification IP

Verification IP (VIP) for MIPI is built upon SystemVerilog UVM-based architecture to provide superior ease-of-use, performance, testbench productivity, and debug to speed and simplify verification of the most complex SoC designs.

VIP for MIPI includes comprehensive test suites which are self-contained and design-proven testbenches. All test suites are delivered in SystemVerilog source code enabling users to easily customize or extend the environment to include unique application-specific tests or corner-case scenarios. Testbench development is accelerated with built-in verification plans, coverage bins, example tests and scenario libraries.

For more information on Synopsys VIP, visit: http://www.synopsys.com/VIP.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired interface IP, wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP Prototyping Kits, IP Virtual Development Kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

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