SYNOPSYS®
Silicon to Software™

DesignWare SuperSpeed USB 3.1 IP

Highlights

- Supports SuperSpeed USB 3.1 at 10 Gbps, SuperSpeed USB 3.0 at 5 Gbps and High-Speed USB (USB 2.0)
- Optimized host, device, and dual-role device controller IP designed to achieve lowest power and area for portable electronics
- DesignWare USB-C 3.1/DisplayPort 1.3 TX PHYs and controllers offer high-performance throughput for 4K and 8K display
- Supports PIPE and UTMI+ PHY interfaces
- Architectural features reduce power consumption
- Complete DesignWare USB solutions for USB 3.1 consist of controllers, PHYs, verification IP, IP Prototyping Kits and IP software development kits
- SuperSpeed USB IP offering from the #1 provider of USB IP for thirteen years in a row (Gartner 2014)

Target Applications

- Smartphones, tablets, ultrabooks
- USB to video display or video display adaptors
- Docking stations
- Storage
- Set-top boxes, smart TVs and digital TVs
- Cloud computing/enterprise and server SoCs

Technology

- Available in leading process technologies through 14/16-nm FinFET

Overview

The DesignWare® SuperSpeed 3.1 USB IP solution is based on the USB 3.0 specification from the USB Implementer Forum. The comprehensive USB 3.1 IP offering consists of host, device, and dual-role device controllers, PHYs with and without support for the USB Type-C™ connectivity specification and DisplayPort 1.3 support, verification IP, IP Prototyping Kits, and IP software development kits. These elements enable quick development of advanced chip designs incorporating the new 10 Gbps SuperSpeed USB standard.

The DesignWare USB 3.1 IP is targeted for integration into SoCs for media storage, creation, and playback devices, requiring faster bandwidth between PCs and portable electronic devices. Optimized for low power, the DesignWare USB 3.1 Controller and PHY IP allow designers to maximize power efficiency for extended battery life. The DesignWare USB 3.1 IP enables the fastest SuperSpeed USB data transfer speeds while lowering overall power consumption.

As the leading supplier of USB IP, Synopsys provides designers with a high-performance, low-power, and area-efficient IP solution, for cost-effective integration into system-on-chip designs. Synopsys' expertise in developing and supporting USB enables us to build a low risk, high quality SuperSpeed USB IP solution.

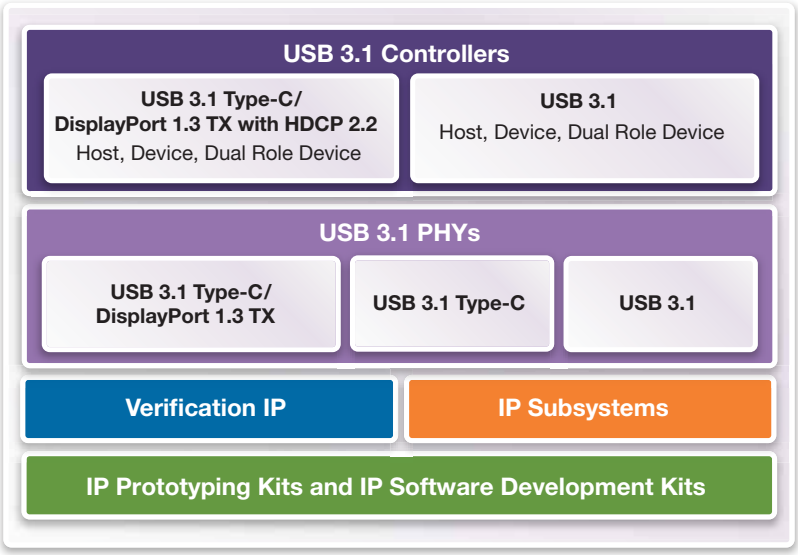

Figure 1. DesignWare USB 3.1 Complete Solution

SuperSpeed USB 3.1 Controller IP

Features

- Lowest risk: Based on proven USB 3.0 controller shipped in 100s of millions of units
- Lowest power: Extend battery life in mobile devices (USB power saving modes, Uniform Power Format, hibernation option with dual power rails)
- Configurable data buffering options to optimize performance vs area
- Supports all USB speed modes
- Host, Device, and Dual Role Device controllers meet the needs for all markets
- USB-C 3.1 DisplayPort 1.3 TX Controller includes HDCP 2.2 content protection

Deliverables

- Synopsys coreConsultant tool
- Verilog RTL source code
- ASIC and FPGA synthesis, ATPG, DFT, power scripts
- UVM Testbench with native SystemVerilog Verification IP for USB
- Comprehensive databook and integration guides
- Reference drivers to speed development
- USB-C 3.1 DisplayPort 1.3 TX Controller includes HDCP 2.2 firmware and host API library SDK

SuperSpeed USB 3.1 PHY IP

Features

- Supports 10 Gbps and 5 Gbps data rates
- x1 and x2 configurations (USB 3.1 PHY only)
- Low active and standby power
- Small area for low silicon cost
- USB Type-C connectivity support available

Deliverables

- GDSII
- LEF
- LIB
- Simulation model
- Testbench
- Databook

Verification IP

Features

- Supports USB 3.1, 3.0, 2.0 and On-The-Go 3.0 and 2.0
- 100% native SystemVerilog
- Host, Device and Hub emulation
- Built-in coverage and verification plan
- Extensive callbacks, messaging, and error injection
- Integrated with Verdi Protocol Analyzer
- Protocol layer
  - Control, interrupt and ISOC
  - Data bursting
  - SS bulk stream
  - LMP, SOF and ITP generation
- Link layer
  - LTSSM with full control to start in any state
  - SS power management

- Cable attach and detach
- Speed fall-back and fall-forward
- Test mode

- PHY layer
  - SS PIPE3, SS serial with clock recovery
  - UTMI, ULPI, SSIC Serial, SSIC RMMI
- Methodology and simulator support
  - UVM, VMM, OVM and Verilog testbenches
  - Supports all major simulators

Deliverables

- VC Verification IP for USB, examples, test sequences

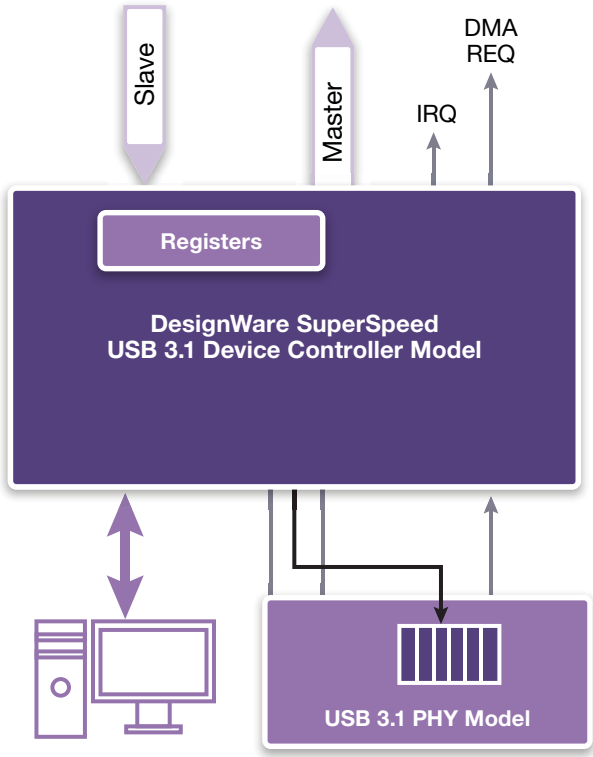

Figure 2. DesignWare IP Virtualizer™ Development Kit for USB 3.1

IP Prototyping Kits

Features

- Provides the essential hardware and software elements needed to reduce IP prototyping and integration effort
- Validated IP configuration can be easily modified using a fast iteration flow to explore design tradeoffs for the target application
- Can be used as proven targets for early software bring-up, debug and test
- Includes pre-instrumented deep-trace debug for most relevant interfaces

Deliverables

- HAPS®-DX FPGA-based prototyping system with pre-configured USB 3.1 Controller IP and SoC integration logic
- System includes USB Type-C connector
- Simulation testbench
- PCI Express® connection to PC

- Linux®-based reference drivers
- FPGA synthesis scripts for high speed interfaces
- Application examples

IP Virtualizer Development Kit

Features

- Provides programmers fast, fully functional models of IP for embedded software driver and application development prior to silicon availability
- Supports a range of debuggers and fits into existing software development flows executing the same binary that can be used on the hardware once available

Deliverables

- DesignWare IP controller models
- Reference virtual prototype
  - Reference Linux® driver
  - VDK software development tools

Interface IP Subsystems

Features

- Configurable, customizable, and pre-validated interface IP subsystems
- Meet critical project schedules by using Synopsys IP protocol and SoC design experts to configure and customize pre-designed USB 3.1 subsystems to unique SoC requirements
- Minimize the subsystem integration effort through the use of pre-validated subsystem and verification tests focused on SoC integration
- Reduce overall development costs while enabling designers to focus on their key competencies

Deliverables

- Pre-configured, pre-validated Synopsys IP for controllers, PHYs and VIP
- Supplemental subsystem logic for clock, reset, DMA, interrupts, and memory maps
- Power management, debug, and testability logic
- Subsystem synthesis and RTL analysis scripts
  - Synthesis timing analysis, CDC checking and linting including rules and constraints for the SoC
- Complete subsystem verification environment that can also be leveraged for SoC verification:
  - Scoreboard, checkers and monitors for easy SoC debug
  - Comprehensive suite of tests that can be reused at SoC level

Third-Party Software Support

Features

- MCCI software drivers and services
- USB 3.0 Host and Device firmware for multiple applications (USB 3.0 SW stack is compatible with USB 3.1 controller and PHY)
- Custom services for multiple applications and operating systems
- USB testing and product services

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired interface IP, wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP Prototyping Kits, IP Virtual Development Kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

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