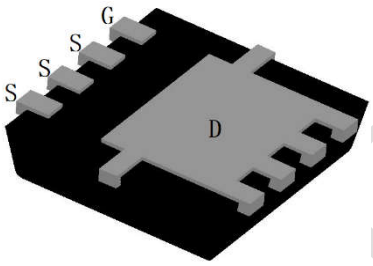
WNM3065

http://www.omnivision-group.com/

Single N-Channel, 30V , 220A ,Power MOSFET

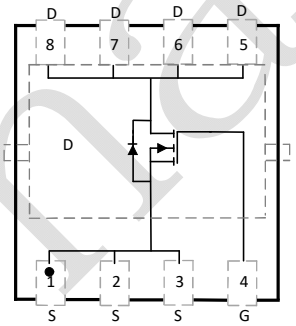
V_{DS} (V)	Max. $R_{DS(on)}$ (mΩ)
30	1.3 @ V_{GS}=10V
	1.8 @ V_{GS}=4.5V



PDFN5X6-8L

Description

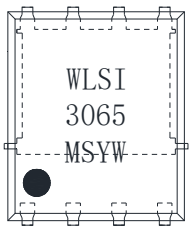
The WNM3065 is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product WNM3065 is in compliance with RoHS.



Pin configuration (Top view)

Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance
- Extremely Low Threshold Voltage
- Package PDFN5X6-8L



3065 = Device Code
MS = Special Code
Y = Year
W = Week(A~z)

Marking

Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
WNM3065-8/TR	PDFN5X6-8L	3000/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C=25°C	I_D	220	A
	T_C=100°C		178	A
Pulsed Drain Current [c]		I_{DM}	TBD	A
Continuous Drain Current [d]	T_A=25°C	I_{DSM}	60	A
	T_A=70°C		48	
Avalanche Energy L=0.3mH		E_{AS}	346	mJ
Power Dissipation [b]	T_C=25°C	P_D	109	W
	T_C=100°C		70	
Power Dissipation [a,d]	T_A=25°C	P_{DSM}	8.1	W
	T_A=70°C		5.2	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	12.9	15.5	°C/W
	Steady State		38.3	46.0	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	0.95	1.14	

Note:

a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm^2 area).

b The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 150°C.

d The power dissipation P_D is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=150°C..

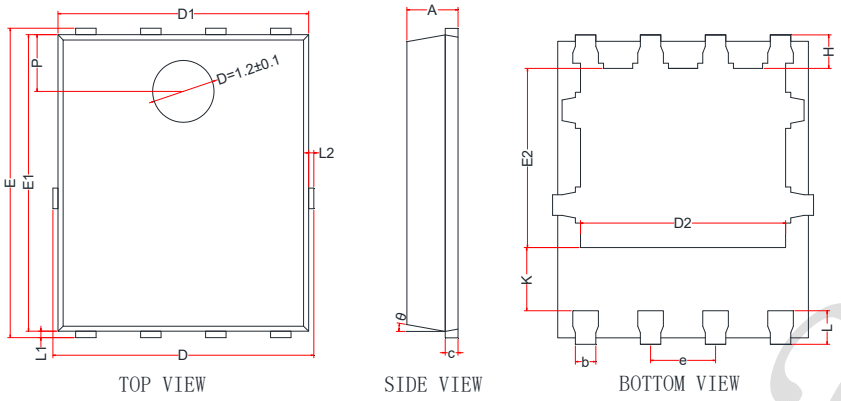
e The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

Electronics Characteristics (Ta=25°C, unless otherwise noted)

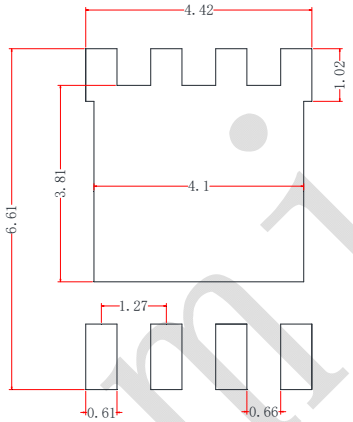
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250uA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V			1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250uA	1.2	1.6	2.2	V
Drain-to-source On-resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A		1.0	1.3	mΩ
		V_{GS} = 4.5V, I_D = 15A		1.3	1.8	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1MHz, V_{DS} = 15 V		6618		pF
Output Capacitance	C_{OSS}			1148		
Reverse Transfer Capacitance	C_{RSS}			696		
Total Gate Charge(V_{GS} = 10 V)	$Q_{G(TOT)}$	V_{DS} = 15 V, I_D = 20 A		125		nC
Total Gate Charge(V_{GS} = 4.5 V)	$Q_{G(TOT)}$			64		
Gate-to-Source Charge	Q_{GS}			19		
Gate-to-Drain Charge	Q_{GD}			25		
Gate Resistance	R_g	f= 1MHz		4		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V_{GS} = 10 V, V_{DS} = 15 V, I_D= 20A , R_G= 5Ω		TBD		ns
Rise Time	tr			TBD		
Turn-Off Delay Time	td(OFF)			TBD		
Fall Time	tf			TBD		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1A		0.65	1	V
Reverse Recovery Time	T_{rr}	I_F=20A,di/dt=100A/us		TBD		ns
Reverse Recovery Charge	Q_{rr}			TBD		nC

PACKAGE OUTLINE DIMENSIONS

PDFN5X6-8L



TOP VIEW　　SIDE VIEW　　BOTTOM VIEW

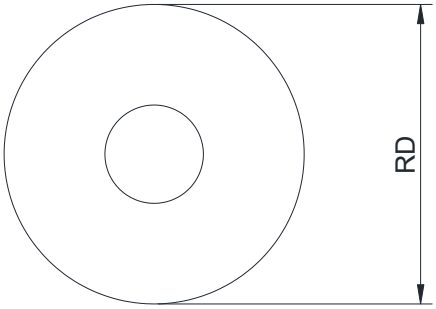


RECOMMENDED LAND PATTERN(Unit:mm)

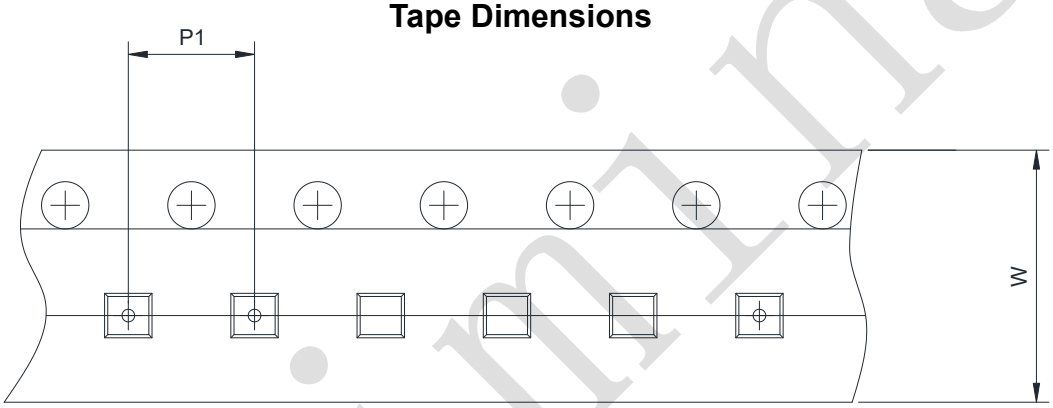
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.90	1.00	1.10
b	0.35	0.40	0.45
c	0.21	0.25	0.34
D	-	-	5.10
D1	4.80	4.90	5.00
D2	3.91	4.01	4.11
e	1.27BSC		
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.375	3.475	3.575
H	0.55	0.65	0.75
K	1.29	-	-
L	0.55	0.65	0.75
L1	0.05	0.15	0.25
L2	-	-	0.12
P	1.00	1.10	1.20
θ	8°	-	12°

TAPE AND REEL INFORMATION

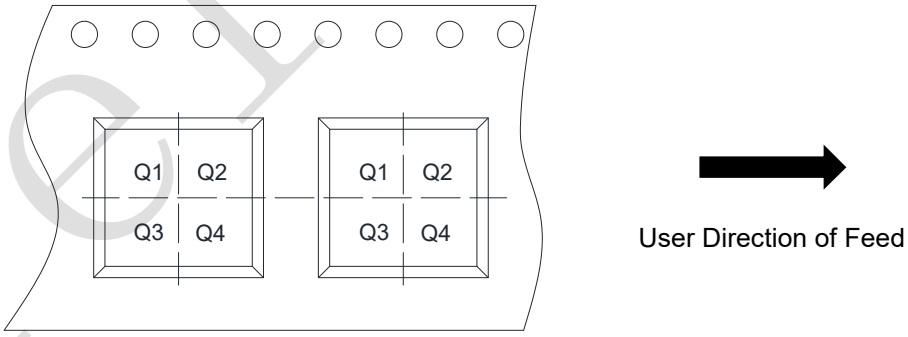
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch	☑ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☑ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm	☑ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4