WS77881L-10/TR

4XSPST（Single-Pole-Single-Throw Switch）

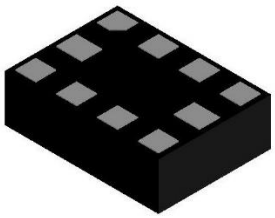


Figure1 LGA1511-10L (Bottom view)

Descriptions

The WS77881L-10/TR is the 4xSPST specifically designed for high performance antenna tuning applications. All RF path performance is enhanced with low on state resistance, low off state capacitance, and ultra high RF voltage handling capability. WS77881L-10/TR allows the creation of advanced tuning topologies to maximize TRP & TIS performance in space constrained applications.

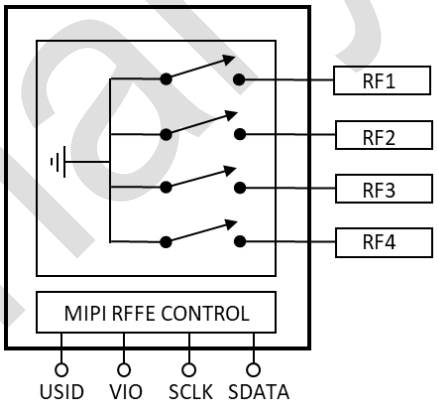


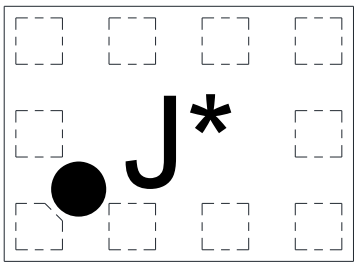
Figure2 Functional Block Diagram

Features

- Ultra High RF voltage handling, >80Vp
- Low On-Resistance, 2.1Ω
- low Off-Capacitance, 110fF
- Very linear performance
- RFFE Control Interface
- 1.5mm x 1.1mm module package
- Single Vio supply, no VDD
- Selectable USID using external pin

Applications

- Antenna Tuning
- Band Switching
- Impedance Tuning



J = Device code

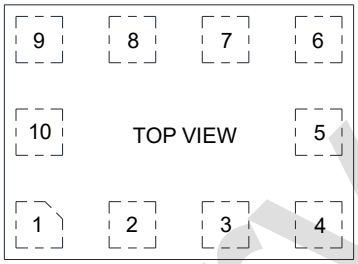
* = Year/Week code（A~Z）

Figure3 Marking (Top view)

Order information

Device	Package	Shipping
WS77881L-10/TR	LGA1511-10L	3000/Reel &Tape

Pin information

Pin	Function	Description	Transparent top view
1	SDATA	RFFE SDATA	
2	SCLK	RFFE SCLK	
3	USID	USID select pin	
4	VIO	VIO supply	
5	GND	Ground	
6	RF4	RF4 Port	
7	RF3	RF3 Port	
8	RF2	RF2 Port	
9	RF1	RF1 Port	
10	GND	Ground	

Application information

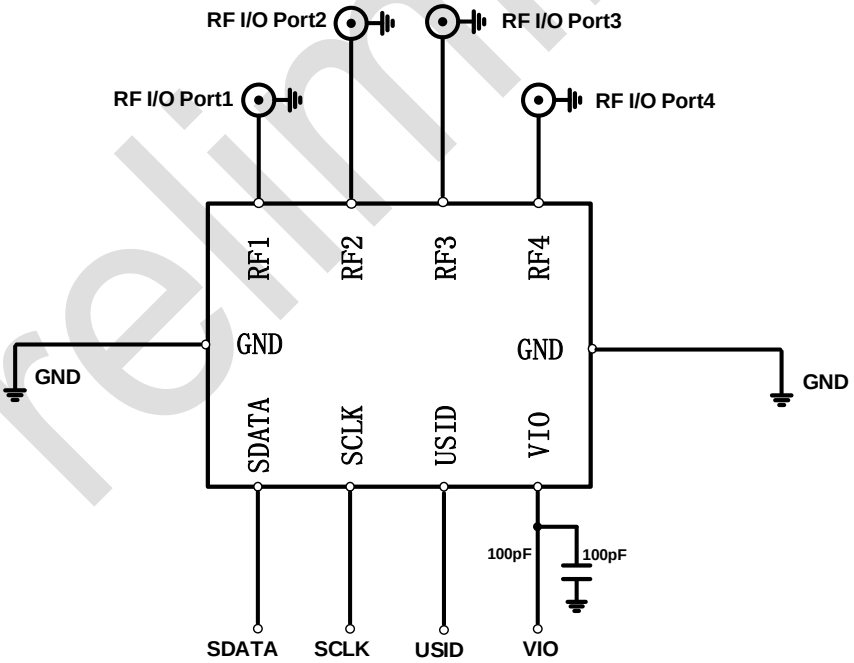


Figure4 Application Circuit

Note1: filter capacitor is needed on VIO.

Absolute maximum ratings

Maximum ratings are absolute ratings, exceeding only one of these values may cause irreversible damage to the integrated circuit.

Parameter	Symbol	Condition	Min.	Max.	Unit
V_{IO}	V_{IO}	T_A=25°C	-0.3	2.5	V
SDATA, SCLK，USID	V_I	T_A=25°C	-0.3	2.5	V
Max RF voltage between RF port and Ground	P_{INMAX}	12.5% Duty cycle, V_{IO}=1.8V, VSWR=6:1, 25°C		83	V
Operating Temperature	T_{OP}		-40	85	°C
Storage Temperature	T_{STG}		-65	150	°C
ESD Capability All Pins	$V_{ESD(HBM)}$	Human Body Model	-2000	+2000	V
	$V_{ESD(CDM)}$	Charged Device Model	-1000	+1000	

Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{IO} Supply Voltage	V_{IO}	1.65	1.8	1.95	V
V_{IO} Supply Current (Active Mode)	I_{VIO}		45		μA
V_{IO} Supply Current (Low Power Mode)	I_{VIO}		4.5	10	μA
SDATA, SCLK Logic Low	V_{IL}	0		0.2 x V_{IO}	V
SDATA, SCLK Logic High	V_{IH}	0.8 x V_{IO}		V_{IO}	V

Characteristics (RF spec)

Nominal test condition unless otherwise stated. All unused ports are 50Ω terminated.
V_{IO}=1.8V, Temp=+25°C, P_{IN}=0dBm, VSWR=1:1, 25°C.

Parameters	Symbol	Conditions	Specifications			Unit
			Min.	Typ.	Max.	
Isolation RF1 - RF3 & RF2 - RF4 OFF-STATE	ISO	617MHz to 915MHz 915MHz to 1910MHz 1910MHz to 2700MHz 3300MHz to 4200MHz 4200 MHz to 5000 MHz 5000 MHz to 6000 MHz 6000 MHz to 7125 MHz		58 53 49 44 40 40 41		dB
Isolation RF1 - RF2 & RF3 - RF4 OFF-STATE	ISO	617MHz to 915MHz 915MHz to 1910MHz 1910MHz to 2700MHz 3300MHz to 4200MHz 4200 MHz to 5000 MHz 5000 MHz to 6000 MHz 6000 MHz to 7125 MHz		34 29 27 23 20 20 21		dB
On Resistance	Ron	Switch Path On		2.1		Ω
Off Capacitance	Coff	Switch Path Off		110		fF
Switching Time - ON	T_{SWON}	From end of RFFE Sequence to 90% of final RF amplitude		10		μs
Switching Time - OFF	T_{SWOFF}	From end of RFFE Sequence to 10% of initial RF amplitude		2		μs
2nd Harmonics (All Ports Off)	HD2	GSM850/900, Pin=35dBm, CW GSM1800/1900, Pin=33dBm, CW		-86 -84		dBm
3rd Harmonics (All Ports Off)	HD3	GSM850/900, Pin=35dBm, CW GSM1800/1900, Pin=33dBm, CW		-75 -79		dBm
2nd Harmonics (One Port Off)	HD2	GSM850/900, Pin=35dBm, CW GSM1800/1900, Pin=33dBm, CW		-88 -85		dBm
3rd Harmonics (One Port Off)	HD3	GSM850/900, Pin=35dBm, CW GSM1800/1900, Pin=33dBm, CW		-86 -88		dBm
RFx Port Off Vpeak	Vpeak	GSM850/900 Tx Band GSM1800/1900 Tx Band	80 80			V

Power ON and OFF sequence

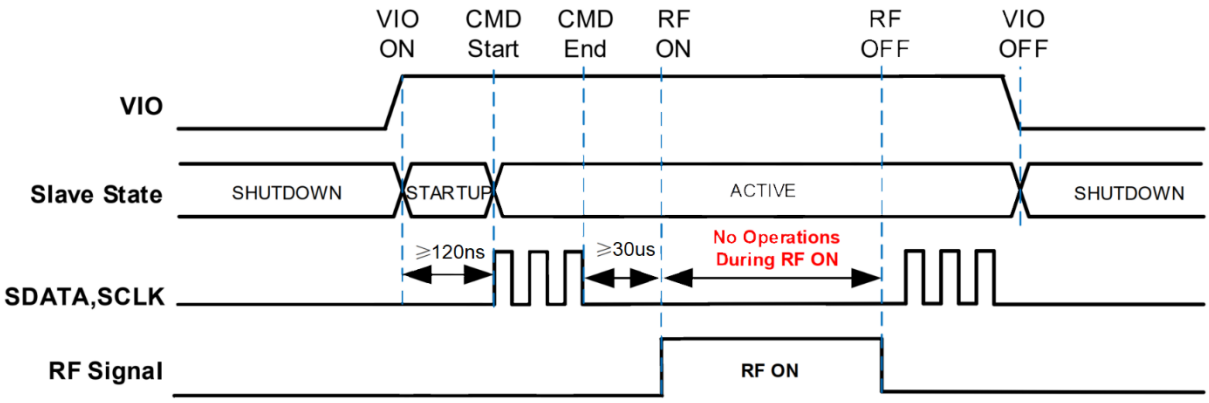
It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device (Note 2).

Power ON

1) Apply voltage supply - VIO
2) Wait 120ns or longer and then apply RFFE – SCLK and SDATA
3) Wait 30μs or longer after RFFE Trigger falling edge and then apply the RF Signal

Power OFF

1) Remove the RF Signal
2) Remove RFFE
3) Remove logic supply – VIO



Note2:

It is important to wait 120ns after VIO is applied before sending SDATA to ensure correction data transmission. It is strongly recommended that no RFFE bus is operated during RF On period to prevent the device from being damaged.

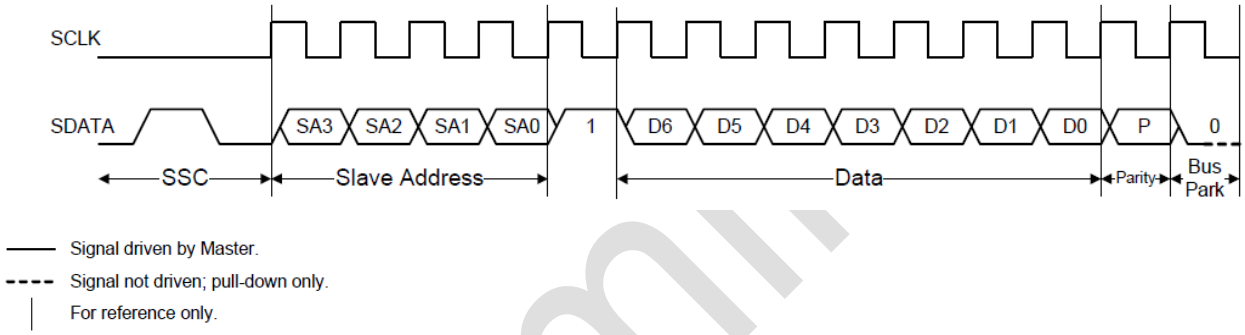
Command Sequence Bit Definitions

Type	SSC	C11-C8	C7	C6-C5	C4	C3-C0	Parity Bits	BPC	Extended Operation					
									DA7(1)-DA0(1)	Parity Bits	BPC	DA7(n)-DA0(n)	Parity Bits	BPC
Reg_0 Write	Y	SA[3:0]	1	Data[6:5]	Data[4]	Data{3:0]	Y	Y	-	-	-	-	-	-
Reg_1 Write	Y	SA[3:0]	0	10	Addr[4]	Data{3:0]	Y	-	Data[7:0]	-	-	-	Y	Y
Reg Read	Y	SA[3:0]	0	11	Addr[4]	Data{3:0]	Y	Y	Data[7:0]	-	-	-	Y	Y

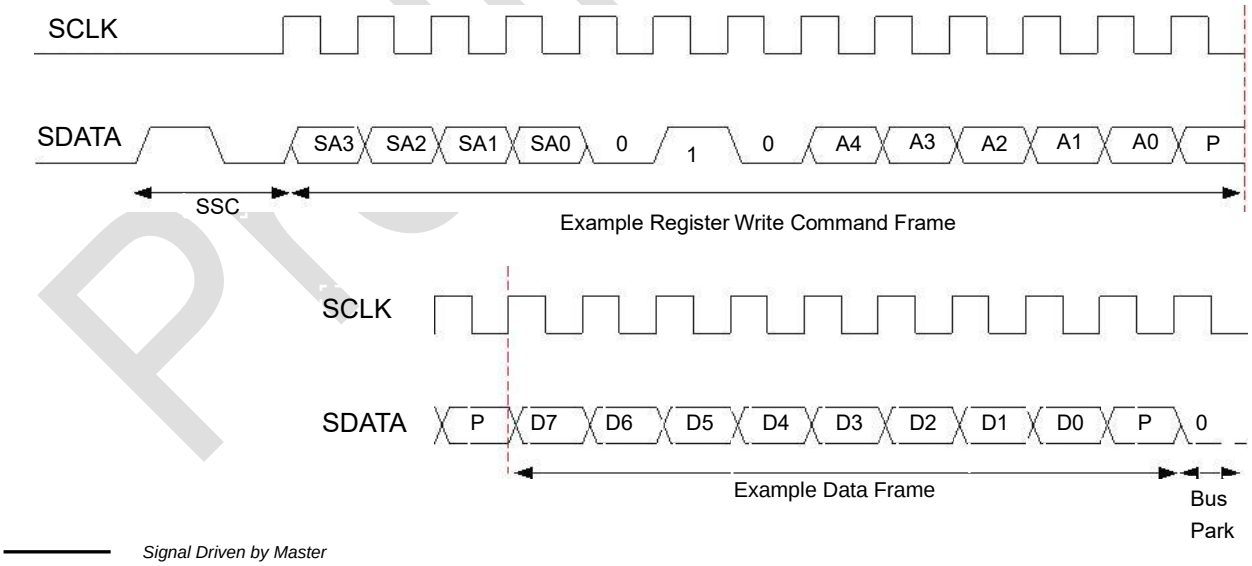
Legend:

SSC = Sequence start command DA = Data/address frame bits BC = Byte count (# of consecutive addresses)

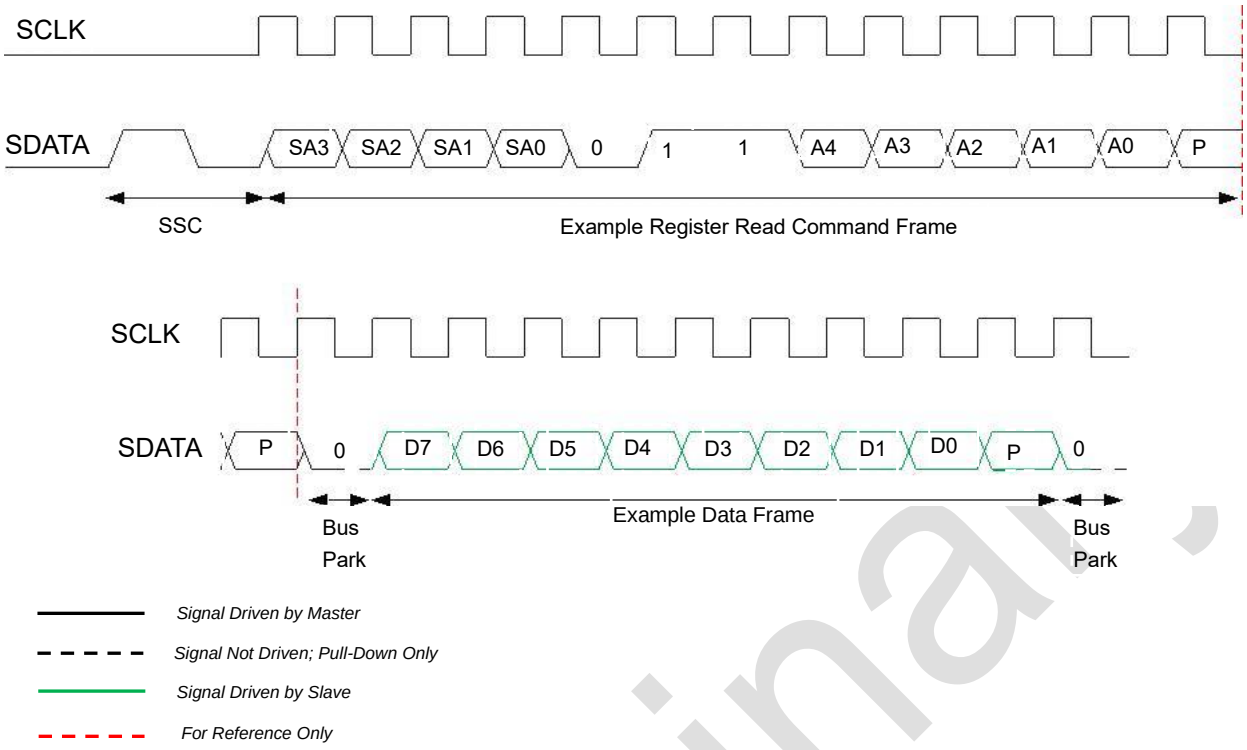
C = Command frame bits BPC = Bus park cycle



Register 0 Write Command Timing Diagram



Register Write Command Timing Diagram



Register Read Command Timing Diagram

Register Truth Table

State	Mode	Register_0							
		D7	D6	D5	D4	D3	D2	D1	D0
1	All ISO	x	x	x	x	0	0	0	0
2	RF1 to GND	x	x	x	x	0	0	0	1
3	RF2 to GND	x	x	x	x	0	0	1	0
4	RF2 & RF1 to GND	x	x	x	x	0	0	1	1
5	RF3 to GND	x	x	x	x	0	1	0	0
6	RF3 & RF1 to GND	x	x	x	x	0	1	0	1
7	RF3 & RF2 to GND	x	x	x	x	0	1	1	0
8	RF3, RF2 & RF1 to GND	x	x	x	x	0	1	1	1
9	RF4 to GND	x	x	x	x	1	0	0	0
10	RF4 & RF1 to GND	x	x	x	x	1	0	0	1
11	RF4 & RF2 to GND	x	x	x	x	1	0	1	0
12	RF4, RF2 & RF1 to GND	x	x	x	x	1	0	1	1
13	RF4 & RF3 to GND	x	x	x	x	1	1	0	0
14	RF4, RF3 & RF1 to GND	x	x	x	x	1	1	0	1
15	RF4, RF3 & RF2 to GND	x	x	x	x	1	1	1	0
16	All to GND	x	x	x	x	1	1	1	1

Register Description and Programming

Register		Parameter	Description	Default
Name	Address			Name
Register_0	0x00	MODE_CTRL	Bits[7:0]: See Register Truth Table for logic	0x00
RFFE_STATUS	0x1A	SOFTWARE RESET	Bits[7]: Resets all data to default values except for USID, GSID, or the contents of the PM_TRIG Register. 0 = Normal operation (active) 1 = Software reset	0b0
		COMMAND_FRAME_PARITY_ERR	Bit[6]: Command sequence received with parity error – discard command.	0b0
		COMMAND_LENGTH_ERR	Bit[5]: Command length error.	0b0
		ADDRESS_FRAME_PARITY_ERR	Bit[4]: Address frame parity error =1.	0b0
		DATA_FRAME_PARITY_ERR	Bit[3]: Data frame with parity error.	0b0
		READ_UNUSED_REG	Bit[2]: Read command to an invalid address.	0b0
		WRITE_UNUSED_REG	Bit[1]: Write command to an invalid address.	0b0
		BID_GID_ERR	Bit[0]: Read command with a BROADCAST_ID (refer to the MIPI Alliance Specification) or GSID.	0b0
GROUP_SID	0x1B	RESERVED	Bits[7:4]: Group Slave ID0.	0x0
		GSID	Bits[3:0]: Group Slave ID1.	0x0
PM_TRIG (Note 3)	0x1C	PWR_MODE	Bits[7:6]: 00 = Normal operation (active) 01 = Default settings (startup) 10 = Low power (low power) 11 = Reserved	0b00
		Trigger_Mask_2	Bit[5]: If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register.	0b0
		Trigger_Mask_1	Bit[4]: If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register.	0b0
		Trigger_Mask_0	Bit[3]: If this bit is set, trigger 0 is disabled. When	0b0

Register		Parameter	Description	Default
Name	Address			Name
			all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register.	
		Trigger_2	Bit[2]: If this bit is set, data is loaded into the trigger 2 registers.	0b0
		Trigger_1	Bit[1]: If this bit is set, data is loaded into the trigger 1 registers.	0b0
		Trigger_0	Bit[0]: If this bit is set, data is loaded into the trigger 0 registers.	0b0
PRODUCT_ID	0x1D	PRODUCT_ID	Bits[7:0]: This is a read-only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed.	0xF9
MANUFAC-TURER_ID	0x1E	MANUFACTURER_ID [7:0]	Bits[7:0]: Read-only register	0xBC
MAN_USID	0x1F	MANUFACTURER_ID [11:8]	Bits[7:4]: Reserved	0b11
		USID	Bits[3:0]: USID pin connected to VIO or floating	0x7
		USID	Bits[3:0]: USID pin connected to GND	0x6

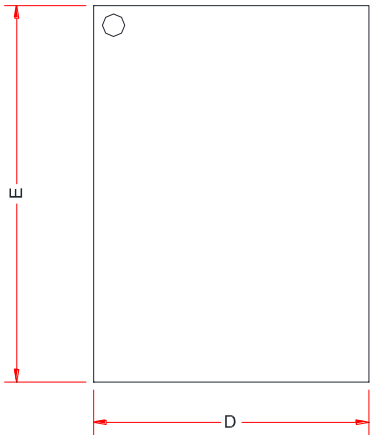
Note3: Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively, as described in the MIPI RFFE Specification this device uses additional interactions between the provided trigger functions.

The delayed application of updated data to all triggerable registers in this device may be accomplished using any of the three triggers (0, 1, or 2), provided that the particular triggerable used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device.

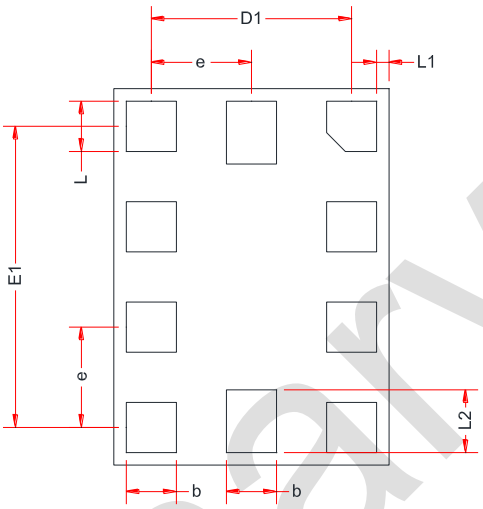
It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register will immediately be written to the destination register at the conclusion of the RFFE command sequence where the data is written.

Package Outline Dimensions

LGA1511-10L

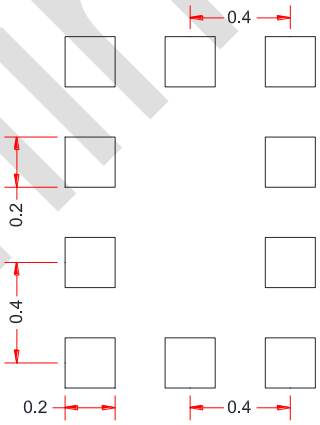


TOP VIEW



BOTTOM VIEW

SIDE VIEW

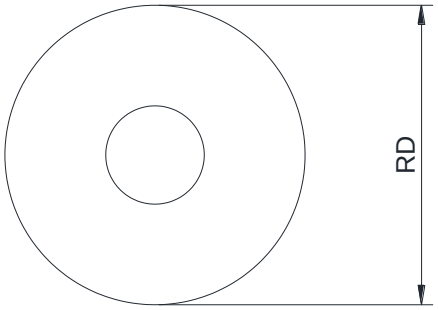


RECOMMENDED LAND PATTERN(unit:mm)

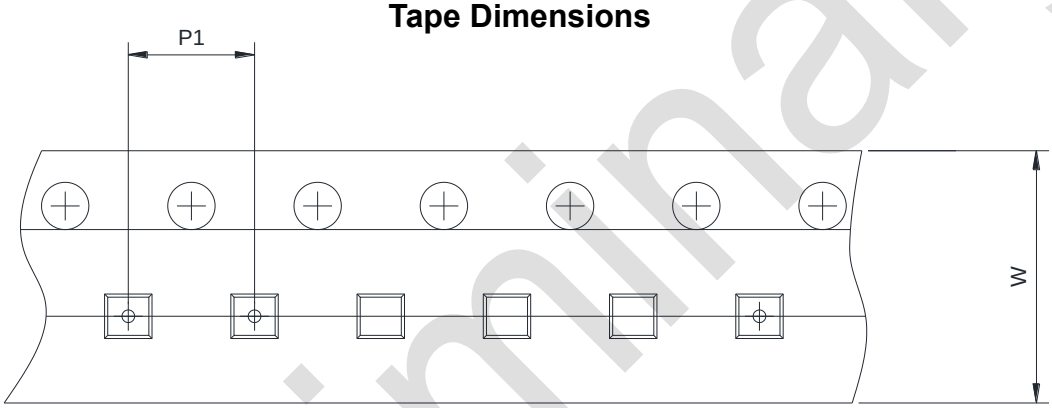
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.41	0.46	0.51
b	0.15	0.20	0.25
L	0.15	0.20	0.25
L1	0.00	0.05	0.10
L2	0.20	0.25	0.30
D	1.05	1.10	1.15
E	1.45	1.50	1.55
D1	0.80 BSC		
E1	1.20 BSC		
e	0.40 BSC		

Tape and Reel Information

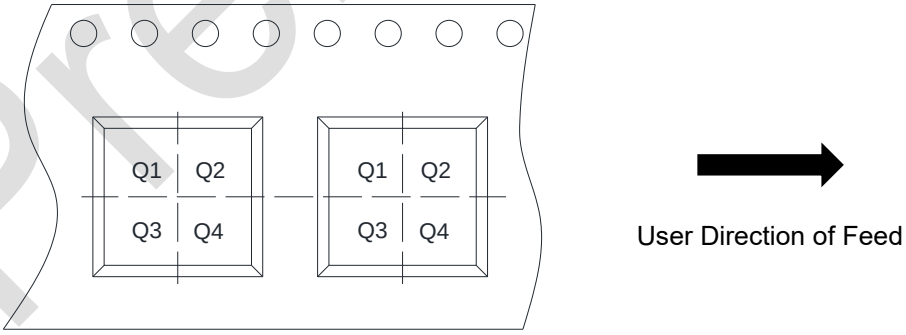
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4