WS7804LMB-12/TR

High Isolation SP4T Switch

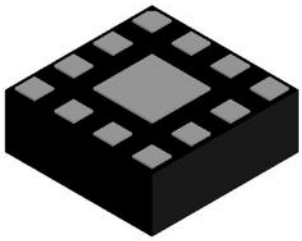


Figure 1 LGA1515-12L (Bottom View)

Descriptions

The WS7804LMB-12/TR is a CMOS-SOI, SP4T switch. The device is optimized for high performance GSM, CDMA, WCDMA, LTE, and 5G_NR applications. All RF path performance is enhanced with low insertion loss, high isolation, and high voltage handling capabilities. The WS7804LMB-12/TR is packaged in a compact 1.5mm×1.5mm, 12-pin module. No external DC blocking capacitors are needed.

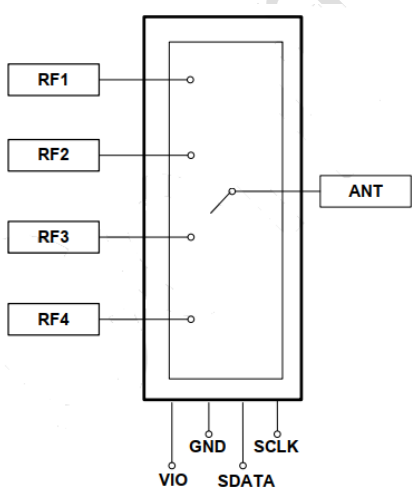


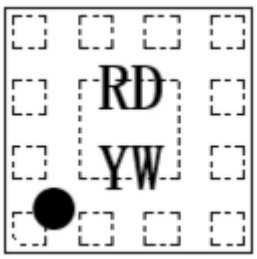
Figure 2 Functional Block Diagram

Features

- Broadband frequency range: 0.4 - 6.0 GHz
- Low insertion loss
- High port-to-port isolation
- RFFE 2.1 control interface
- Small 1.5 mm×1.5 mm, LGA package

Applications

- Cell Handset Applications
- Cell Modems and USB Devices
- Multi-Mode GSM, EDGE, WCDMA, LTE, and 5G_NR Applications



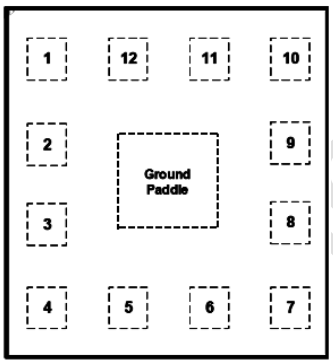
RD = Device code
YW = Month code（A~Z）

Figure 3 Marking (Top View)

Order Information

Device	Package	Shipping
WS7804LMB-12/TR	LGA1515-12L	3000/Tape&Reel

Pin Information

Pin	Function	Description	Transparent Top View
1	ANT	Antenna input/output	
2	GND	Ground	
3	RF1	RF I/O path 1	
4	GND	Ground	
5	RF3	RF I/O path 3	
6	VIO	MIPI Interface/reference voltage	
7	SDATA	Data input/output	
8	SCLK	Clock signal	
9	RF4	RF I/O path 4	
10	GND	Ground	
11	RF2	RF I/O path 2	
12	GND	Ground	

Application Information

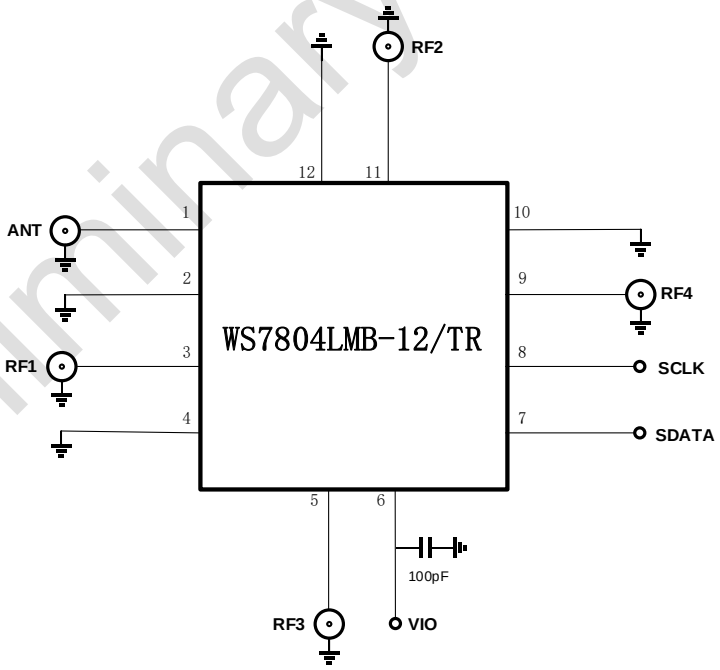


Figure 4 Application Circuit

Absolute Maximum Ratings

Maximum ratings are absolute ratings. Exceeding any of these values might cause irreversible damage to the integrated circuit.

Parameter	Symbol	Condition	Min.	Max.	Unit
V_{IO}	V_{IO}	T_A=25°C	-0.3	2.5	V
SDATA, SCLK	V_I	T_A=25°C	-0.3	2.5	V
Maximum Input Power	P_{INMAX}	400~6000 MHz		34	dBm
Operating Temperature	T_{OP}		-40	85	°C
Storage Temperature	T_{STG}		-55	150	°C
ESD Capability All Pins	$V_{ESD(HBM)}$	Human Body Model	1000		V
	$V_{ESD(CDM)}$	Charged Device Model	500		

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{IO} Supply Voltage	V_{IO}	1.6	1.8	2.0	V
V_{IO} Supply Current (Active Mode)	I_{VIO}		70	100	μA
V_{IO} Supply Current (Low Power Mode)	I_{VIO}			10	μA
SDATA, SCLK Logic Low	V_{IL}	0		0.2 x V_{IO}	V
SDATA, SCLK Logic High	V_{IH}	0.8 x V_{IO}		V_{IO}	V
Switch Time	T_{SW}		1	2	μs

Characteristics (RF spec)

Nominal test condition unless otherwise stated. All unused ports are 50Ω terminated. Vio = 1.8 V, Temp = +25°C.

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Insertion Loss （ANT to RFx）	IL	400~ 1000 MHz 1000~2200 MHz 2200~2700 MHz 3400~3800 MHz 4000~5000 MHz 5000~6000 MHz		0.45 0.50 0.55 0.60 0.65 0.70		dB
Isolation （ANT to RFx）	ISO	400~ 1000 MHz 1000~2200 MHz 2200~2700 MHz 3400~3800 MHz 4000~5000 MHz 5000~6000 MHz		53 46 45 44 42 40		dB
Isolation （RFx to RFx）	ISO	400~ 1000 MHz 1000~2200 MHz 2200~2700 MHz 3400~3800 MHz 4000~5000 MHz 5000~6000 MHz		52 46 44 42 41 41		dB
Input Return Loss	RL	400~6000 MHz		10		dB
Input 0.1dB compression point [1]	P0.1dB	400~6000 MHz		30		dBm
2nd Harmonic	HD2	F=915 MHz, Pin=26 dBm		-70		dBm
3rd Harmonic	HD3			-60		dBm
2nd Harmonic	HD2	F=1910 MHz, Pin=26 dBm		-70		dBm
3rd Harmonic	HD3			-60		dBm

Note1: Defined at the RF input power at which either 2fo or 3fo harmonic reaches -40 dBm with VSWR = 1.

Register Definition

Register Address	Register Name	Data Bits	R/W	Function	Description	Default	BROADCAST_ID support	Trigger support
0x00	REGISTER_0	7:0	R/W	RF Control	Register_0 truth Table	0x00	No	Yes
0x1A	RFFE_STATUS	7	R/W	SOFTWARE RESET	0b0: Normal operation 0b1: Software reset	0b0	No	No
					Note: On software reset, this register and all configurable registers are reset except for USID, GSID, and PM_TRIG.			
		6	R/W	COMMAND_FRAME_PARITY_ERR	Command Frame with parity error	0b0	No	No
		5	R/W	COMMAND_LENGTH_ERR	Command Sequence with incorrect length	0b0	No	No
		4	R/W	ADDRESS_FRAME_PARITY_ERR	Address Frame with parity error	0b0	No	No
		3	R/W	DATA_FRAME_PARITY_ERR	Data Frame with parity error	0b0	No	No
		2	R/W	READ_UNUSED_REG	Read Command Sequence to an invalid address	0b0	No	No
		1	R/W	WRITE_UNUSED_REG	Write Command Sequence to an invalid address	0b0	No	No
		0	R/W	BID_GID_ERR	Read Command Sequence with a BSID or GSID Note: Reading this register resets this register	0b0	No	No
0x1B	GROUP_SID	7:4	R	RESERVED		0x0	No	No
		3:0	R/W	GSID	Group Slave ID	0x0	No	No
0x1C	PM_TRIG	7:6	R/W	PWR_MODE	00: ACTIVE– Normal Operation 01: STARTUP –Reset all registers to default settings 10: ACTIVE – Low Power 11: STARTUP –Reset all registers to default settings	0b10	Yes	No
		5:3	R/W	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed	0b000	No	No
		2:0	W	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers	0b000	Yes	No
0x1D	PRODUCT_ID	7:0	R	PRODUCT_ID	Product Number	0x17	No	No

Register Address	Register Name	Data Bits	R/W	Function	Description	Default	BROADCAST_ID support	Trigger support
0x1E	MANUFACTURER_ID	7:0	R	MANUFACTURER_ID[7:0]	Lower eight bits of MIPI registered Manufacturer ID	0xBC	No	No
0x1F	MAN_USID	7:6	R	RESERVED		0b00	No	No
		5:4	R	MANUFACTURER_ID[9:8]	Upper two bits of MIPI registered Manufacturer ID	0b11	No	No
		3:0	R/W	USID	Unique Slave Address	0x8	No	No

Register_0 Truth Table for RF Operating Modes

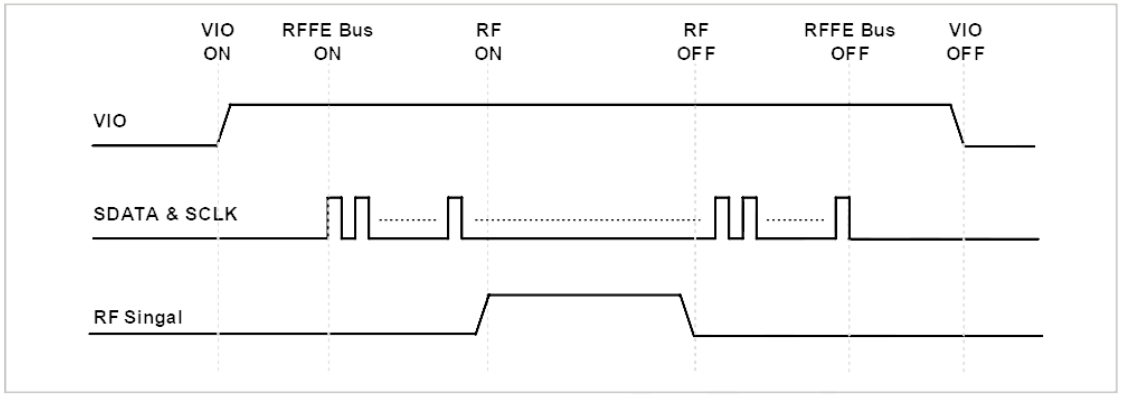
State	Value(Hex)	Mode	Register Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
1	0x00	ALL OFF(Isolation)	x	x	x	x	x	x	x	x
2	0x01	RF1 ON	x	x	x	x	x	x	x	1
3	0x02	RF2 ON	x	x	x	x	x	x	1	x
4	0x04	RF3 ON	x	x	x	x	x	1	x	x
5	0x08	RF4 ON	x	x	x	x	1	x	x	x
6	0x10	ALL OFF(Isolation) With 50 Ohm termination	x	x	x	1	x	x	x	x

MIPI RFFE Operating Sequences

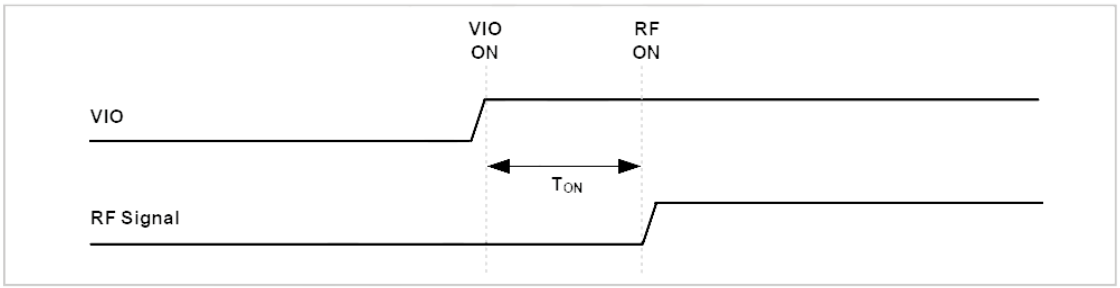
Here are some recommendations for MIPI RFFE operating sequences to prevent the device from damage.

1) Basic Operational Sequences

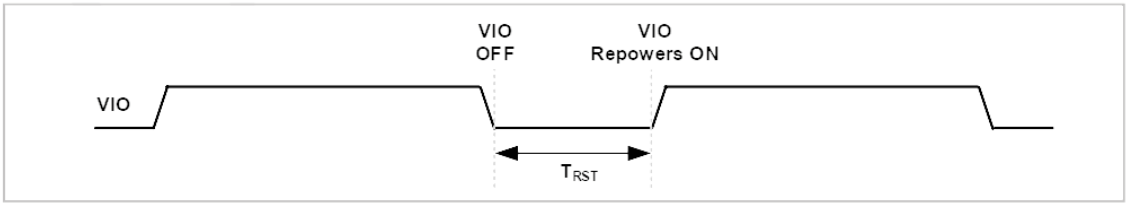
- Power On -- Apply Supply (VIO)-> Apply MIPI RFFE Bus (SCLK & SDATA) -> Apply RF Signal
- Power Off -- Remove RF Signal-> Remove MIPI RFFE Bus (SCLK & SDATA)->Remove Supply (VIO)



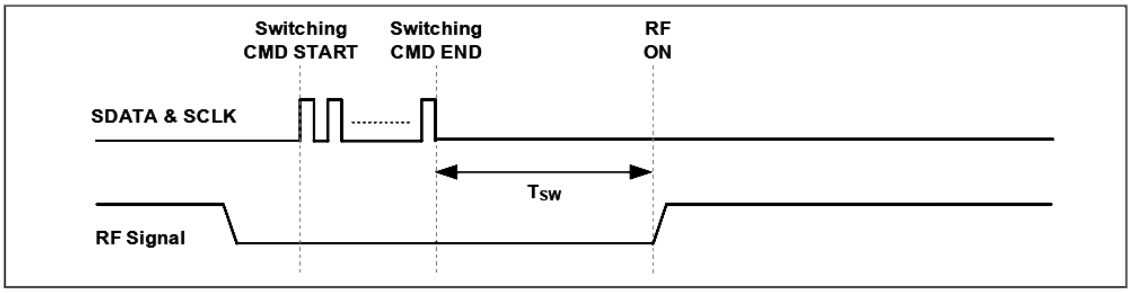
2) There shall be at least T_{ON} before RF power can be applied to any RF Path.



3) Once VIO is off, there shall be at least T_{RST} before VIO is allowed to power on again.

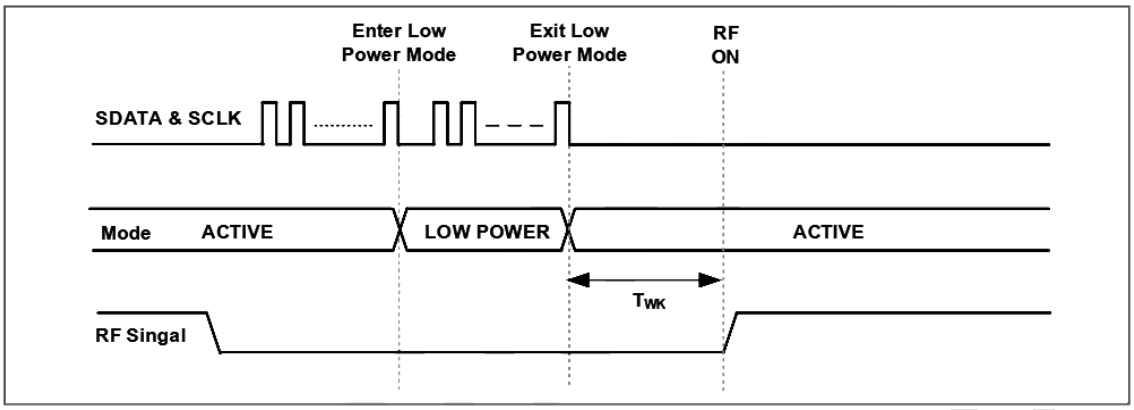


4) If RF signal is to be switched from one RF path to another or some paths to others, RF signal shall not be applied during such switching events to protect the devices. Hence, RF signal shall be removed before the switching command is implemented. RF signal shall not be applied before waiting at least T_{SW}.



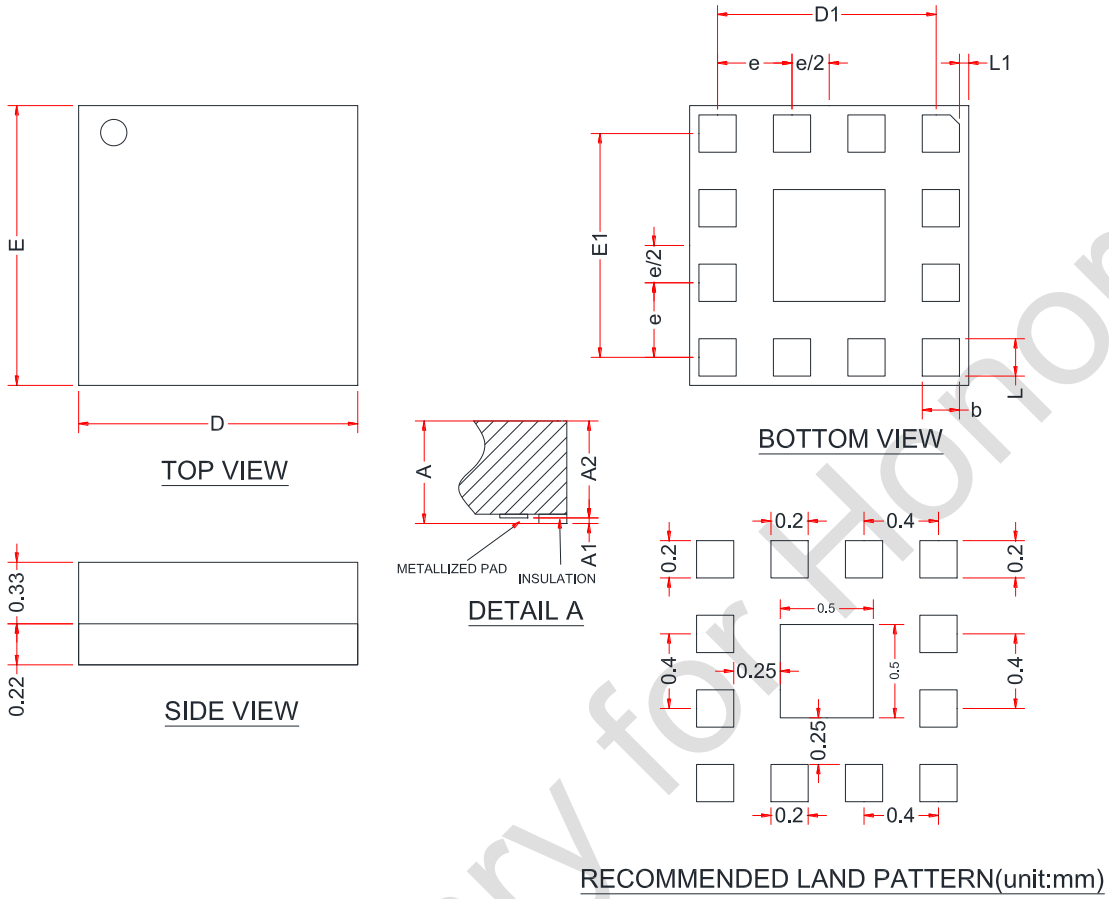
5) RF Signal shall not be applied during low power state. Hence, RF signal shall be removed before device

enters low power state. After the state is switched from low power to active, there shall be at least T_{WK} before the RF signal can be applied.



Package Outline Dimensions

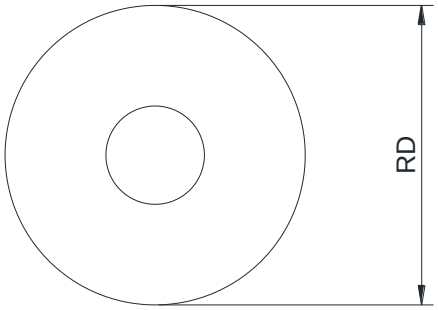
LGA1515-12L



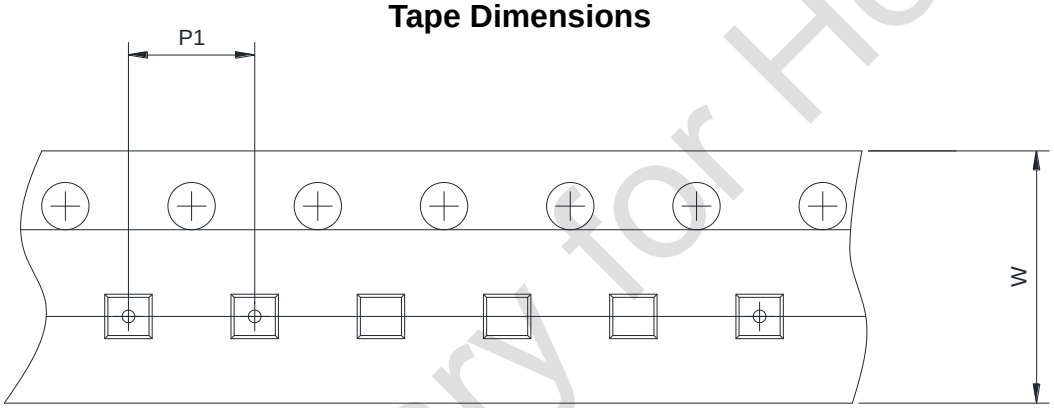
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A1	0.00	--	0.03
A2	--	--	0.57
b	0.15	0.20	0.25
L	0.15	0.20	0.25
D	1.45	1.50	1.55
E	1.45	1.50	1.55
D1	1.20 BSC		
E1	1.20 BSC		
e	0.40 BSC		
L1	0.00	0.05	0.10

Tape and Reel Information

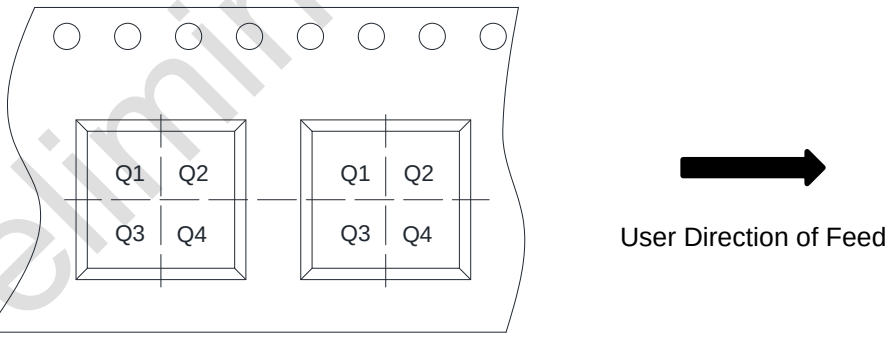
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4