WS7824LMB-16/TR

617MHz to 5000MHz DP4T Switch with MIPI RFFE Interface

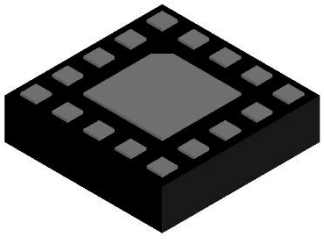


Figure 1 LGA2x2-16L (Bottom view)

Descriptions

The WS7824LMB-16/TR is a low loss, high linearity dual-pole four-throw (DP4T) switch with performance optimized for transfer routing applications.

The WS7824LMB-16/TR integrates a serial control system compatible with the RFFE standard. The select lines (SID) provide USID addressability and up to two placements of the WS7824LMB-16/TR on the same RFFE Bus. The WS7824LMB-16/TR runs off a single VIO voltage supply.

The WS7824LMB-16/TR is manufactured in a compact 2.0x2.0x0.55mm, 16-pin LGA package.

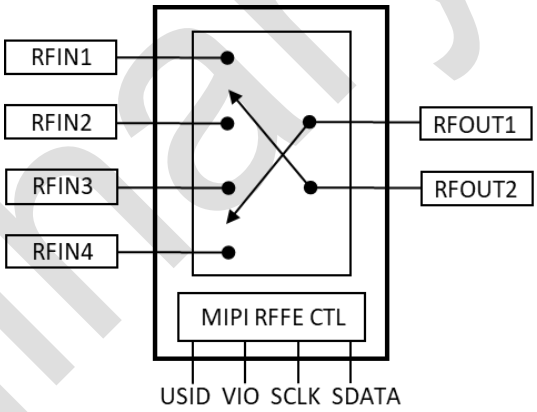


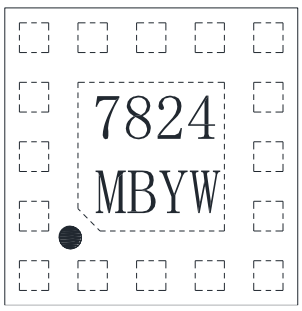
Figure 2 Functional Block Diagram

Features

- Multi-Band operation: 617 to 5000MHz
- Excellent Insertion Loss and Isolation performance
- High Linearity
- RFFE 2.1 Control Interface
- DC blocking capacitors are not required in typical applications

Applications

- Cellular Handset Applications
- Multi-Mode GSM, CDMA, WCDMA,LTE and NR including n77, n78, n79 frequency bands



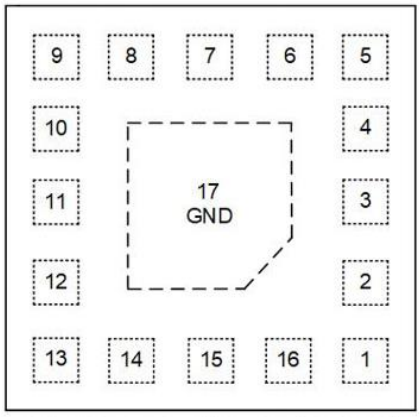
7824 = Device code
MB = Special code
YW = Year/Week code

Figure 3 Marking (Top View)

Order Information

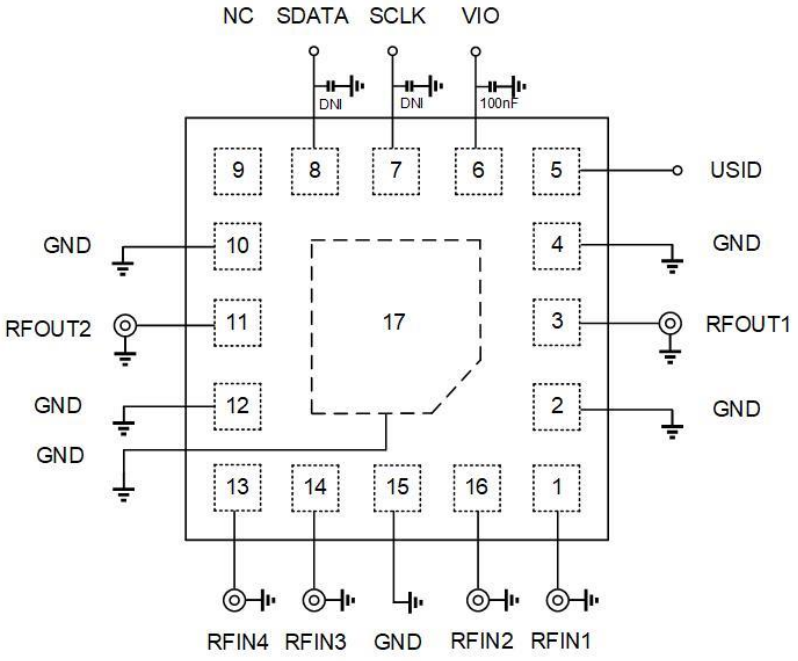
Device	Package	Shipping
WS7824LMB-16/TR	LGA2x2-16L	3000/Tape&Reel

Pin information

Pin	Function	Description	Transparent top view
1	RFIN1	RF Input Port1	 (Top view)
2	GND	Ground	
3	RFOUT1	RF Output Port1	
4	GND	Ground	
5	USID	USID Select Pin	
6	VIO	RFFE Power Supply	
7	SCLK	RFFE Clock Signal	
8	SDATA	RFFE Data Signal	
9	NC	No connection	
10	GND	Ground	
11	RFOUT2	RF Output Port2	
12	GND	Ground	
13	RFIN4	RF Input Port4	
14	RFIN3	RF Input Port3	
15	GND	Ground	
16	RFIN2	RF Input Port2	
17	GND	Ground	

Note 1: Bottom ground paddles must be connected to ground.

Application information



Note2: filter capacitor is needed on VIO respectively.

Absolute maximum ratings

Maximum ratings are absolute ratings, exceeding only one of these values may cause irreversible damage to the integrated circuit.

Parameter	Symbol	Condition	Min.	Max.	Unit
V_{IO}	V_{IO}	T_A=25°C	-0.3	2.5	V
SDATA, SCLK	V_I	T_A=25°C	-0.3	2.5	V
Maximum Input Power	P_{INMAX}	12.5% Duty cycle, VSWR=1:1, 25°C		40	dBm
Operating Temperature	T_{OP}		-40	85	°C
Storage Temperature	T_{STG}		-65	150	°C
ESD Capability All Pins	$V_{ESD(HBM)}$	Human Body Model	1000		V
	$V_{ESD(CDM)}$	Charged Device Model	500		

Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{IO} Supply Voltage	V_{IO}	1.65	1.8	1.95	V
V_{IO} Supply Current (Active Mode)	I_{VIO}		75		μA
V_{IO} Supply Current (Low Power Mode)	I_{VIO}		2.5	10	μA
SDATA, SCLK Logic Low	V_{IL}	0		0.2 x V_{IO}	V
SDATA, SCLK Logic High	V_{IH}	0.8 x V_{IO}		V_{IO}	V

Characteristics (RF spec)

Nominal test condition unless otherwise stated. All unused ports are 50Ω terminated.
VIO=1.8V, Temp=+25°C, P_{IN} =0dBm.

Parameters	Symbol	Conditions	Specifications			Unit
			Min.	Typ.	Max.	
Insertion Loss (RFINx to RFOUTy)	IL	617MHz to 960MHz 1425MHz to 2200MHz 2300MHz to 2690MHz 3300MHz to 3800MHz 3800MHz to 4200MHz 4400MHz to 5000MHz		0.42 0.50 0.55 0.70 0.80 1.00		dB
Isolation (Dual Through Mode, No-Adjacent Ports)	ISO	617MHz to 960MHz 1425MHz to 2200MHz 2300MHz to 2690MHz 3300MHz to 3800MHz 3800MHz to 4200MHz 4400MHz to 5000MHz		43 36 34 32 31 30		dB
Isolation (Dual Through Mode, Adjacent Ports)	ISO	617MHz to 960MHz 1425MHz to 2200MHz 2300MHz to 2690MHz 3300MHz to 3800MHz 3800MHz to 4200MHz 4400MHz to 5000MHz		38 31 30 27 26 25		dB
Input Return Loss (RFINx to RFOUTy)	RL	617MHz to 2200MHz 2300MHz to 5000MHz		20 10		dB
Second Harmonics (RFINx to RFOUTy)	HD2	F_0 =915MHz , P_{IN}=+35dBm F_0 =1910MHz , P_{IN}=+33dBm F_0 =2600MHz , P_{IN}=+26dBm F_0 =3800MHz , P_{IN}=+26dBm F_0 =5000MHz , P_{IN}=+26dBm		-65 -72 -71 -71 -71		dBm
Third Harmonics (RFINx to RFOUTy)	HD3	F_0 =915MHz , P_{IN}=+35dBm F_0 =1910MHz , P_{IN}=+33dBm F_0 =2600MHz , P_{IN}=+26dBm F_0 =3800MHz , P_{IN}=+26dBm F_0 =5000MHz , P_{IN}=+26dBm		-55 -60 -80 -74 -72		dBm
Input 0.1dB Compression Point (RFINx to RFOUTy)	P0.1dB	0.7GHz to 2.7GHz，CW		38		dBm
IIP2	IIP2	F_0 =1950MHz , P_{IN}=+20dBm F_1 =4090MHz , P_{IN}=-15dBm		125		dBm
IIP3	IIP3	F_0 =1950MHz , P_{IN}=+20dBm F_1 =1760MHz , P_{IN}=-15dBm		67		dBm
VSWR	VSWR	617MHz to 960MHz 1425MHz to 2200MHz		1.09 1.18		

		2300MHz to 2690MHz 3300MHz to 3800MHz 3800MHz to 4200MHz 4400MHz to 5000MHz		1.24 1.39 1.43 1.52		
Switching Time - ON	T_{STON}+ T_{UP}	From end of RFFE Sequence to 90% of final RF amplitude		3		μs
Switching Time - OFF	T_{DOWN}	From end of RFFE Sequence to 10% of initial RF amplitude		1.5		μs

Power ON and OFF sequence

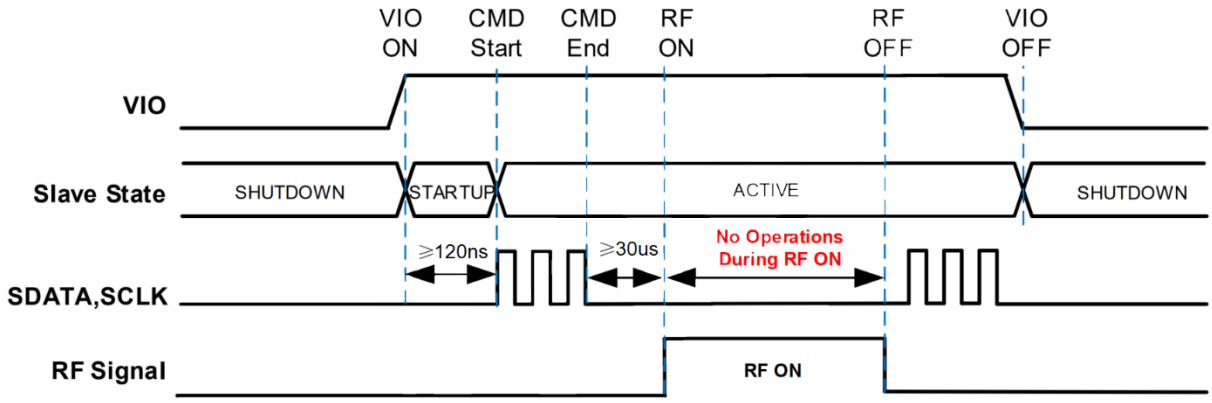
It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device (Note 2).

Power ON

1) Apply voltage supply - VIO
2) Wait 120ns or longer and then apply RFFE – SCLK and SDATA
3) Wait 30μs or longer after RFFE Trigger falling edge and then apply the RF Signal

Power OFF

1) Remove the RF Signal
2) Remove RFFE
3) Remove logic supply – VIO



Note2:

It is important to wait 120ns after VIO is applied before sending SDATA to ensure correction data transmission. It is strongly recommended that no RFFE bus is operated during RF On period to prevent the device from being damaged.

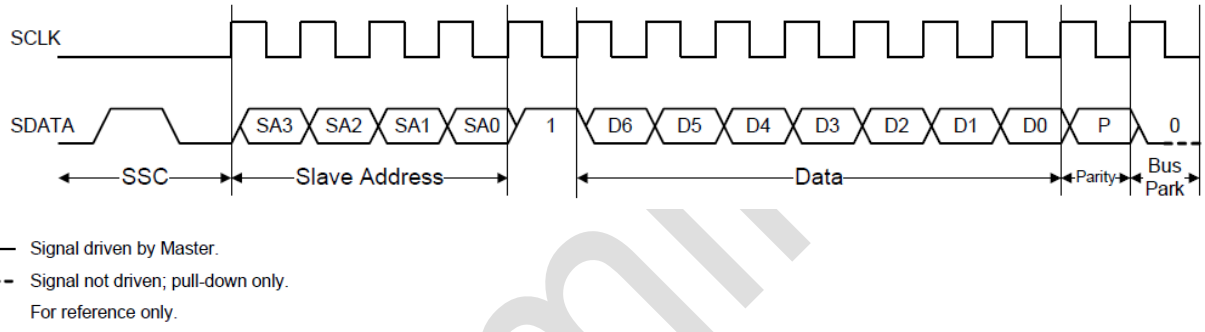
Command Sequence Bit Definitions

Type	SSC	C11-C8	C7	C6-C5	C4	C3-C0	Parity Bits	BPC	Extended Operation					
									DA7(1)-DA0(1)	Parity Bits	BPC	DA7(n)-DA0(n)	Parity Bits	BPC
Reg_0 Write	Y	SA[3:0]	1	Data[6:5]	Data[4]	Data[3:0]	Y	Y	-	-	-	-	-	-
Reg_1 Write	Y	SA[3:0]	0	10	Addr[4]	Data[3:0]	Y	-	Data[7:0]	-	-	-	Y	Y
Reg Read	Y	SA[3:0]	0	11	Addr[4]	Data[3:0]	Y	Y	Data[7:0]	-	-	-	Y	Y

Legend:

SSC = Sequence start command DA = Data/address frame bits BC = Byte count (# of consecutive addresses)

C = Command frame bits BPC = Bus park cycle

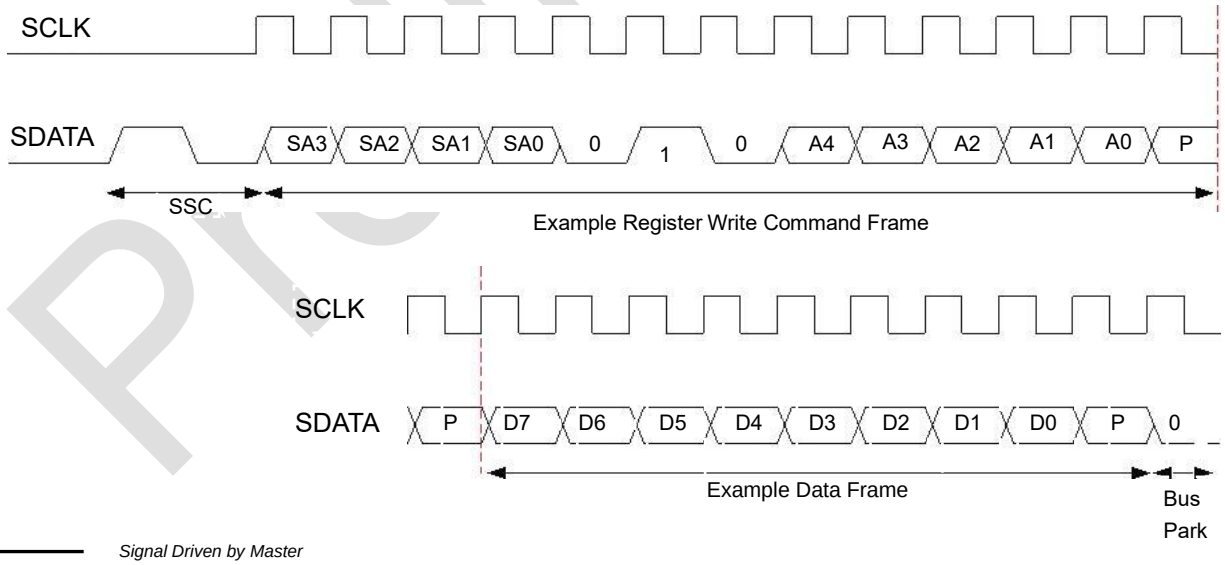


Signal driven by Master.

Signal not driven; pull-down only.

For reference only.

Register 0 Write Command Timing Diagram

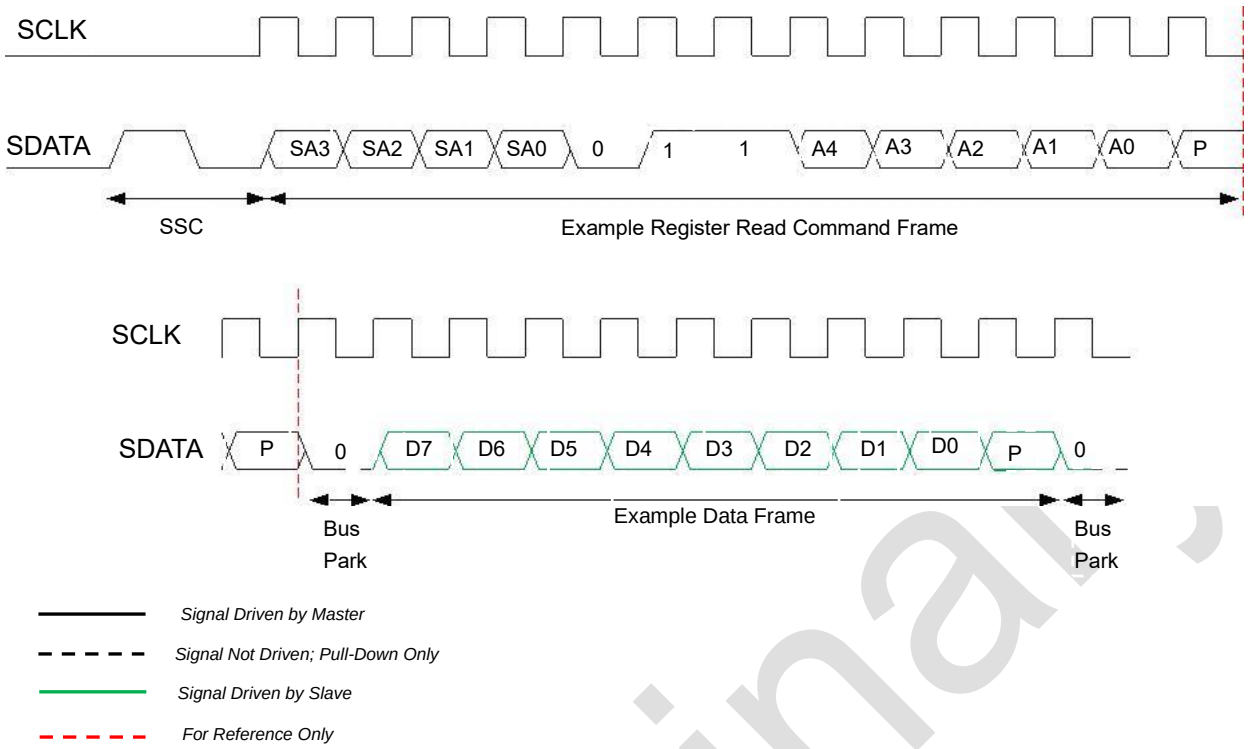


Signal Driven by Master

Signal Not Driven; Pull-Down Only

For Reference Only

Register Write Command Timing Diagram



Register Read Command Timing Diagram

Register Mapping

Register0	Output Switching Control Register							
Patch	D7	D6	D5	D4	D3	D2	D1	D0
Direct Mode	x	x	x	x	x	X	x	0
Cross Mode	x	x	x	x	x	X	x	1

Register Truth Table (Register0[0] = 0)

State	Mode (Register0[0]=0)		Register1							
	RFOUT1	RFOUT2	D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation	Isolation	x	x	0	0	0	0	0	0
2	RFIN1	Isolation	x	x	0	0	0	0	0	1
3	RFIN2	Isolation	x	x	0	0	0	0	1	0
4	RFIN3	Isolation	x	x	0	0	0	1	0	0
5	RFIN4	Isolation	x	x	0	0	1	0	0	0
6	RFIN1	RFIN2	x	x	0	1	0	0	1	1
7	RFIN1	RFIN3	x	x	0	1	0	1	0	1
8	RFIN2	RFIN3	x	x	0	1	0	1	1	0
9	RFIN1	RFIN4	x	x	0	1	1	0	0	1
10	RFIN2	RFIN4	x	x	0	1	1	0	1	0
11	RFIN3	RFIN4	x	x	0	1	1	1	0	0
12	RFIN2	RFIN1	x	x	1	0	0	0	1	1
13	RFIN3	RFIN1	x	x	1	0	0	1	0	1
14	RFIN3	RFIN2	x	x	1	0	0	1	1	0
15	RFIN4	RFIN1	x	x	1	0	1	0	0	1
16	RFIN4	RFIN2	x	x	1	0	1	0	1	0
17	RFIN4	RFIN3	x	x	1	0	1	1	0	0
18	Isolation	RFIN1	x	x	1	1	0	0	0	1
19	Isolation	RFIN2	x	x	1	1	0	0	1	0
20	Isolation	RFIN3	x	x	1	1	0	1	0	0
21	Isolation	RFIN4	x	x	1	1	1	0	0	0

Register Truth Table (Register0[0] = 1)

State	Mode (Register0[0]=1)		Register1							
	RFOUT1	RFOUT2	D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation	Isolation	x	x	0	0	0	0	0	0
2	Isolation	RFIN1	x	x	0	0	0	0	0	1
3	Isolation	RFIN2	x	x	0	0	0	0	1	0
4	Isolation	RFIN3	x	x	0	0	0	1	0	0
5	Isolation	RFIN4	x	x	0	0	1	0	0	0
6	RFIN2	RFIN1	x	x	0	1	0	0	1	1
7	RFIN3	RFIN1	x	x	0	1	0	1	0	1
8	RFIN3	RFIN2	x	x	0	1	0	1	1	0
9	RFIN4	RFIN1	x	x	0	1	1	0	0	1
10	RFIN4	RFIN2	x	x	0	1	1	0	1	0
11	RFIN4	RFIN3	x	x	0	1	1	1	0	0
12	RFIN1	RFIN2	x	x	1	0	0	0	1	1
13	RFIN1	RFIN3	x	x	1	0	0	1	0	1
14	RFIN2	RFIN3	x	x	1	0	0	1	1	0
15	RFIN1	RFIN4	x	x	1	0	1	0	0	1
16	RFIN2	RFIN4	x	x	1	0	1	0	1	0
17	RFIN3	RFIN4	x	x	1	0	1	1	0	0
18	RFIN1	Isolation	x	x	1	1	0	0	0	1
19	RFIN2	Isolation	x	x	1	1	0	0	1	0
20	RFIN3	Isolation	x	x	1	1	0	1	0	0
21	RFIN4	Isolation	x	x	1	1	1	0	0	0

Register Description and Programming

Register		Parameter	Description	Default Name
Name	Address (Hex)			
Register_0	0x00	Output_Cross_CTRL	Bits[7:1]: Reserved for future use.	0b0000000
			Bit[0]: 0 = DPDT Direct operating mode 1 = DPDT output cross operating mode	0b0
Register_1	0x01	SW_CTRL	Bits[7:6]: Reserved for future use.	0b00
			Bits[5:0]: See Register Truth Table for logic	0b000000
RFFE_STATUS	0x1A	SOFTWARE RESET	Bits[7]: Resets all data to default values except for USID, GSID, or the contents of the PM_TRIG Register. 0 = Normal operation (active) 1 = Software reset	0b0
		COMMAND_FRAME_PARITY_ERR	Bit[6]: Command sequence received with parity error – discard command.	0b0
		COMMAND_LENGTH_ERR	Bit[5]: Command length error.	0b0
		ADDRESS_FRAME_PARITY_ERR	Bit[4]: Address frame parity error =1.	0b0
		DATA_FRAME_PARITY_ERR	Bit[3]: Data frame with parity error.	0b0
		READ_UNUSED_REG	Bit[2]: Read command to an invalid address.	0b0
		WRITE_UNUSED_REG	Bit[1]: Write command to an invalid address.	0b0
		BID_GID_ERR	Bit[0]: Read command with a BROADCAST_ID (refer to the MIPI Alliance Specification) or GSID.	0b0
GROUP_SID	0x1B	RESERVED	Bits[7:4]: Group Slave ID0.	0b0000
		GSID	Bits[3:0]: Group Slave ID1.	0b0000
PM_TRIG (Note 4)	0x1C	PWR_MODE	Bits[7:6]: 00 = Normal operation (active) 01 = Default settings (startup) 10 = Low power (low power) 11 = Reserved	0b00
		Trigger_Mask_2	Bit[5]: If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register.	0b0
		Trigger_Mask_1	Bit[4]: If this bit is set, trigger 1 is disabled. When	0b0

Register		Parameter	Description	Default Name
Name	Address (Hex)			
			all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register.	
		Trigger_Mask_0	Bit[3]: If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register.	0b0
		Trigger_2	Bit[2]: If this bit is set, data is loaded into the trigger 2 registers.	0b0
		Trigger_1	Bit[1]: If this bit is set, data is loaded into the trigger 1 registers.	0b0
		Trigger_0	Bit[0]: If this bit is set, data is loaded into the trigger 0 registers.	0b0
PRODUCT_ID	0x1D	PRODUCT_ID	Bits[7:0]: This is a read-only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed.	0xA0
MANUFAC-TURER_ID	0x1E	MANUFACTURER_ID [7:0]	Bits[7:0]: Read-only register	0xBC
MAN_USID	0x1F	MANUFACTURER_ID [11:8]	Bits[7:4]: Reserved	0b0011
		USID	Bits[3:0]: USID pin connected to VIO	0xA
			Bits[3:0]: USID pin connected to GND	0xB

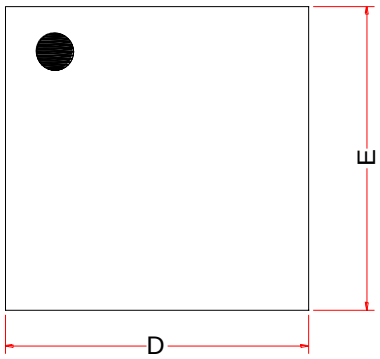
Note4: Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively, as described in the MIPI RFFE Specification this device uses additional interactions between the provided trigger functions.

The delayed application of updated data to all triggerable registers in this device may be accomplished using any of the three triggers (0, 1, or 2), provided that the particular triggerable used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device.

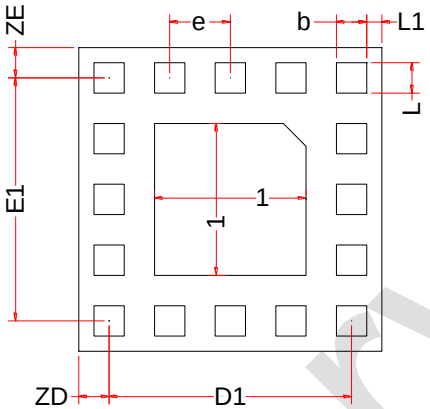
It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register will immediately be written to the destination register at the conclusion of the RFFE command sequence where the data is written.

Package Outline Dimensions

LGA2X2-16L

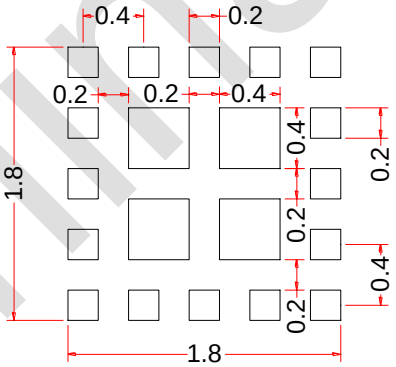


TOP VIEW



BOTTOM VIEW

SIDE VIEW

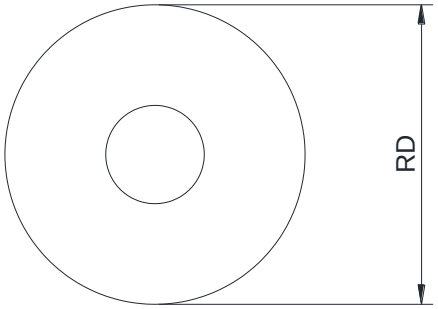


RECOMMENDED LAND PATTERN(unit:mm)

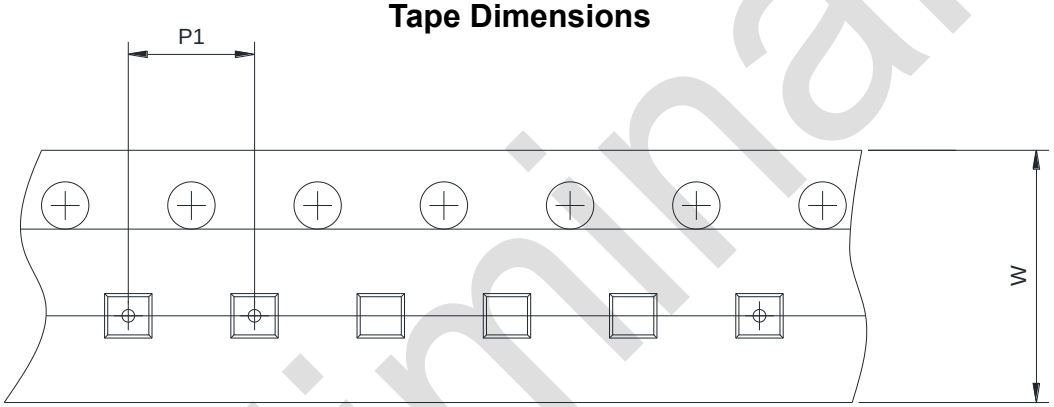
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.48	0.55	0.62
b	0.15	0.20	0.25
L	0.15	0.20	0.25
D	1.95	2.00	2.05
E	1.95	2.00	2.05
D1	1.60 BSC		
E1	1.60 BSC		
ZD	0.20BSC		
ZE	0.20BSC		
e	0.40 BSC		
L1	0.00	0.10	0.20

Tape and Reel Information

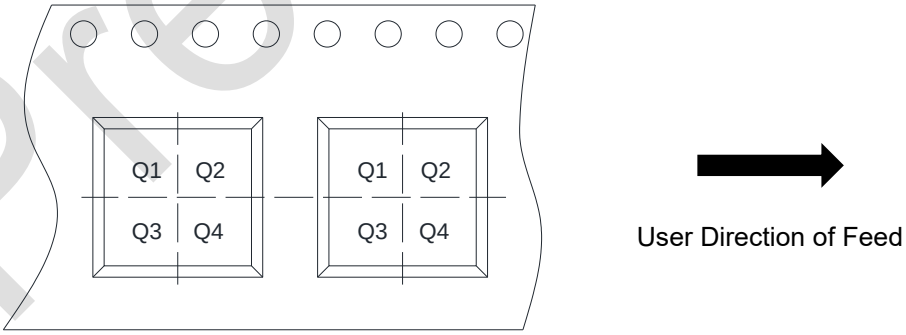
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4