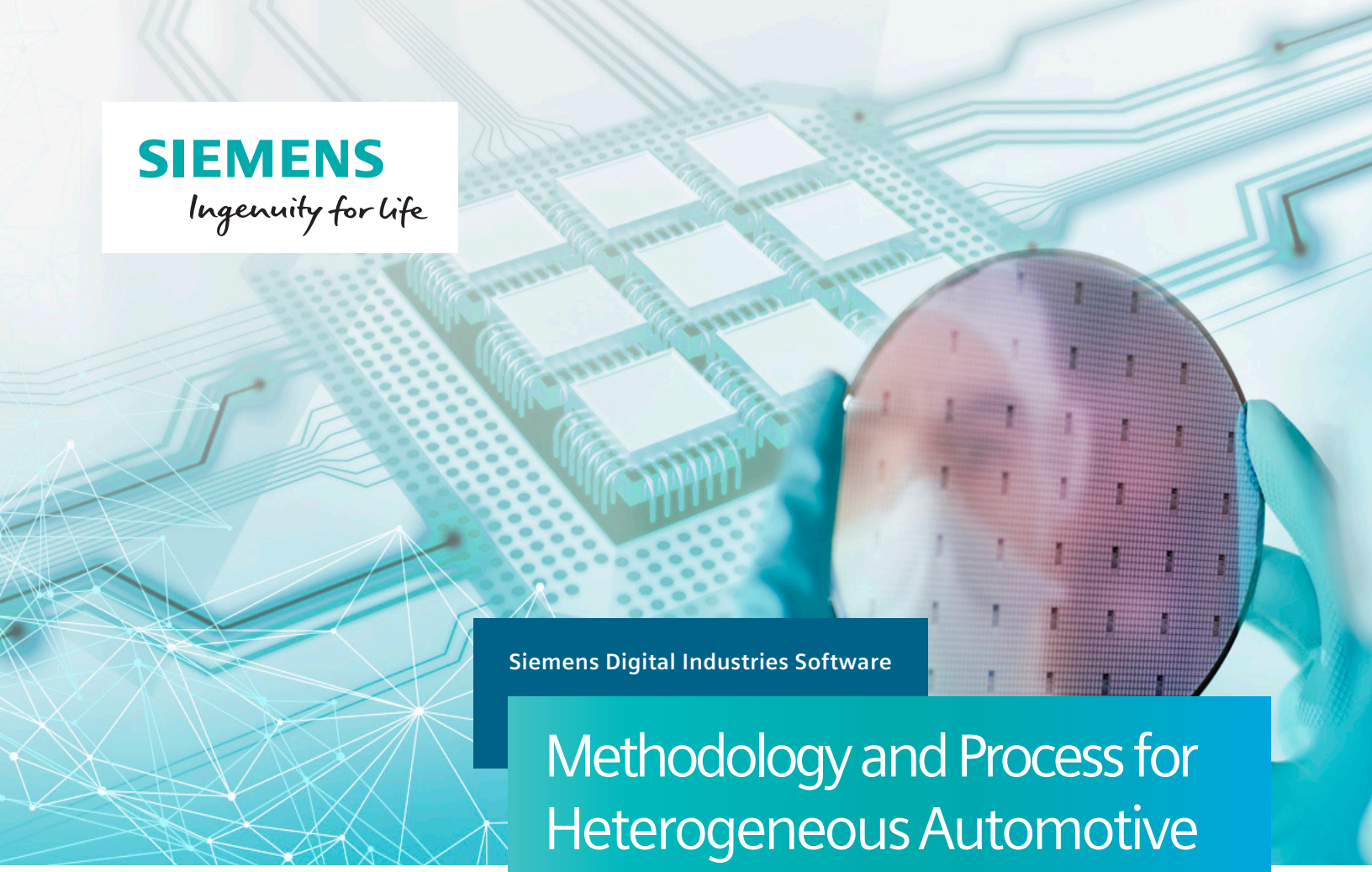

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Methodology and Process for Heterogeneous Automotive Package Design

Executive summary

This paper explains why the STMicroelectronics Back-End Manufacturing Technology R&D team selected Xpedition Substrate Integrator (xSI) from Siemens EDA to support connectivity optimization in their next high-end automotive co-design project.

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Introduction

As a leading supplier of automotive semiconductors, STMicroelectronics must continue to move fast to develop and deliver leading-edge solutions. Employing package design as part of system innovation requires the STMicroelectronics Back-End Manufacturing Technology R&D organization to embrace the key driving forces of product development.

In the automotive field, package designers need to explore new methodologies and adopt a specific co-design flow for IC-package connectivity-data exchange (such as netlist tables) that is data robust and flexible. The STMicroelectronics Back-End Manufacturing Technology R&D team located in Agrate, Italy adopted Xpedition Substrate Integrator (xSI) from Siemens EDA, a part of Siemens Digital Industries Software, to help design activity meet these needs.

Automotive packaging challenges

With the massive growth of electronics in the automotive sector (such as autonomous driving, electric vehicles, and safety systems), the complexity, capabilities, and volume of semiconductors is rapidly increasing the demand for greater package connectivity density. This has led to high-end IC-package solutions, such as copper pillar bumping with very fine pitches for flip chip applications. Furthermore, the move towards more in-package silicon integration using complex configurations, and the requirement to improve substrate stack-up with an increasing number of metal layers to meet performance specifications, make configurations and system iterations much more complex.

Within this context, the approach to design must include an in-depth assessment, starting with early-stage feasibility analysis, to investigate and predict early electrical performance in order to drive package development, selection and technology.

ADAS as an example

Advanced driver-assistance systems (ADAS) are pervasive today in almost all new vehicles on the market, and their level of capabilities continues to increase, requiring higher semiconductor integration, performance, and bandwidth while producing smaller overall device form factors. Figure 1 shows an example of bump-out evolution for automotive applications.

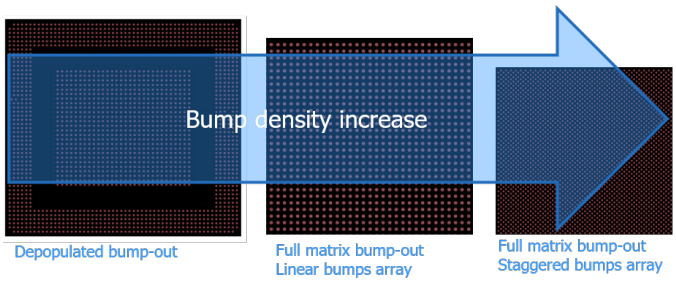

Figure 1: Bump-out evolution for automotive applications.

The impact on package design is considerable including, but not limited to, the following:

Challenge Area	Trends
Bump pitch	< 120 µm
Bump density	> 50 bumps/mm^2
Bump-out configuration	full matrix and staggered
Ball pitch	< 0.8 mm
Current consumption	> 50 Amps
Electrical challenges	Huge growing frequencies of high-speed interfaces (DDR, PCIe, MIPI)

Automotive design approach

To support automotive product development, a package design flow must be well-structured across each of the three macro stages described below.

Early Stage

Here the focus is on design rules identification, implementation technology, cost optimization and design strategy validation. In this stage the design team explores through prototyping and planning the package dimension, design technology, and substrate stack-up definition. Specific areas of investigation include bump and ball out definition, breakout strategies and preliminary connectivity assignment, innovative techniques for ensuring specification uniformity, and trial or preliminary implementation for detailed performance and cost estimation.

Intermediate Stage

This stage focuses on physical design, debugging, and optimization. The main activities are around substrate routing finalization and optimization, manufacturability readiness, early assessment of critical interfaces, and modeling and optimization of specific power demand—such as core supply DC drop—to prepare the design for the finalization stage and reduce overall validation cycle time.

Final Stage

In this last stage the focus is on electrical/thermal performance and manufacturability verification. Activities include comparison against signal integrity and power integrity target values, system-level power integrity analysis, final manufacturing verification and signoff, and, finally, tape-out handoff to manufacturing.

All three of these design stages have a fundamental dependency for co-design, co-simulation, and co-optimization at the system level, which means, in this context, at the entire device assembly level.

Best design practice

To support the above approach for automotive, high-end design, there must be a transition from a component-level to a system-level focus that incorporates die, package, and system PCB. A system-level approach enables optimization of system connectivity and performance through the usage of co-design and co-simulation techniques.

Challenges of Current Approach at the Early Stage

At the early stage of automotive package development, design teams focus on three major, strictly-connected areas for preparing package decisions, improving co-design productivity, and making iteration loops among design teams more efficient. The first challenge is to evaluate and validate the preliminary die floorplan with particular attention to connectivity issues, such as high-speed interface bump assignments and power and ground bump placement and pitch. The second is to define the packaging technology that meets the devices cost and performance goals. Often the technology evaluation must establish if the reuse of an existing, stable technology is the right approach, or if a new technology is more appropriate for that specific application. The third challenge is to include and analyze customer constraints in terms of ball assignment to achieve electrical target specifications and system requirements.

The IC-Package-PCB information exchange is often complex to handle during the early design stage because data is produced in several formats that depend on several factors, such as level of data maturity, customer flows, and source of information. Spreadsheets for data exchange are a common format, but they are not always ready in the early stage for package and die creation. It makes handling data exchanges prone to mistakes and time consuming during the data update from and to different system design groups.

This use of spreadsheets must change: a faster way for analyzing bump and ball connectivity and supporting what if analysis is needed for the overall system view and optimization. Figure 2 shows connectivity table examples for IC and BGA devices and the package view inside the Siemens Xpedition Substrate Integrator (xSI) tool.

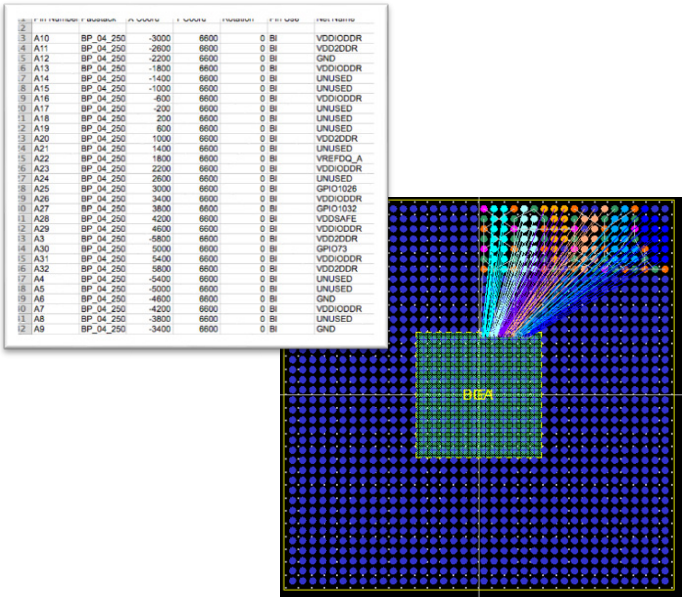

Figure 2: Connectivity tables for IC and BGA devices and the package view inside Xpedition Substrate Integrator (xSI).

Evaluation Drivers for Early Feasibility Analysis

In a robust co-design flow, the handling of complex device data as designs evolve is supported by an efficient automation solution that allows more flexible feasibility analysis. The key to evaluation is the ability to integrate a prototyping tool into the current package design flow to facilitate communication across design teams. It needs to be flexible in data management and allow designers to create devices or components from scratch with the flexibility to handle complex bump and ball pitch and positions. It should also provide routing optimization and optimization capabilities for supporting fast connectivity updates and reuse of any specifications on the current or next design. Other evaluation "nice-to-haves" include the support of a systems approach as well as tight integration with layout tools that support bidirectional routing optimization.

ST evaluated the Siemens Xpedition Substrate Integrator (xSI) to see if it could address their early-stage issues and provide a solution for their co-design requirements. They found that it did, so the ST team in Agrate adopted it. Among other things, xSI allows designers to quickly create and evaluate ball and bump pattern scenarios, and it provides the capabilities to plan, manage, optimize, and visualize the entire system-level connectivity from die to package to system PCBs.

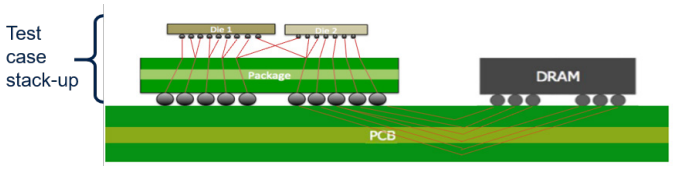

Figure 3: A typical automotive heterogeneous package assembly.

The evaluation test case

The test case design we used to evaluate the xSI solution was based on future development. It included a BGA with 1620 balls, a logic die with a full matrix, complex, staggered, bump-pitch configuration integrating multiple DDR interfaces that required connectivity planning and IC-package-PCB optimization for system performance achievement. Partial connectivity was provided as tables with power, ground, and signal rules for bump and ball assignments. Starting from the physical creation of the devices, a preliminary bump-to-ball connectivity list was planned, based on IO ring sequence and substrate stack-up strategy, and design rules were selected. The definition of a robust environment allowed an easier data update and modification as the design and project evolved. Figure 4 shows the connectivity list that is implemented on it.

Example of P/G/S assignment

Connectivity

Ball Name	Fucntional Name
DDR0_DQ_A1	DDR0_DQ_A[1]
DDR0_DQ_A2	DDR0_DQ_A[2]
DDR0_DQ_A3	DDR0_DQ_A[3]
DDR0_DQ_A4	DDR0_DQ_A[4]
DDR0_DQ_A5	DDR0_DQ_A[5]
DDR0_DQ_A6	DDR0_DQ_A[6]
DDR0_DQ_A7	DDR0_DQ_A[7]
DDR0_DQ_A8	DDR0_DQ_A[8]
DDR0_DQ_A9	DDR0_DQ_A[9]
DDR0_DQ_A10	DDR0_DQ_A[10]
DDR0_DQ_A11	DDR0_DQ_A[11]
DDR0_DQ_A12	DDR0_DQ_A[12]
DDR0_DQ_A13	DDR0_DQ_A[13]
DDR0_DQ_A14	DDR0_DQ_A[14]
DDR0_DQ_A15	DDR0_DQ_A[15]
DDR0_DMI_A0	DDR0_DMI_A[0]
DDR0_DMI_A1	DDR0_DMI_A[1]
DDR0_RDQS_T_A0	DDR0_RDQS_T_A[0]
DDR0_RDQS_T_A1	DDR0_RDQS_T_A[1]
DDR0_RDQS_C_A0	DDR0_RDQS_C_A[0]
DDR0_RDQS_C_A1	DDR0_RDQS_C_A[1]
DDR0_WCK_T_A0	DDR0_WCK_T_A[0]
DDR0_WCK_T_A1	DDR0_WCK_T_A[1]

Figure 4: A bump-out assignment and its connectivity list implementation. Bump colors represent package nets assignment.

Results and conclusions

xSI allows system netlist construction and management for heterogeneous packages, aggregation of data from multiple sources in multiple formats, and visualization and interaction of all interconnect levels from a single environment. It provides hierarchical construction of the complete package assembly with step-by-step handling of multiple parts, including reuse of parts.

Based on high-speed interface connectivity planning and optimization and multi-pitch bump-out evaluation, xSI provides:

- Flexibility for IC-package connectivity planning and optimization
- Efficient integration with external tools
- Fluid and fast on command response
- Very good technical support from the Siemens EDA team

For these reasons, the STMicroelectronics Back-End Manufacturing Technology R&D located in Agrate, Italy selected xSI to support connectivity optimization in their next high-end automotive co-design project.

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About the author

Cristina Somma is a Package Development Senior Engineer working at STMicroelectronics in the Back-End Manufacturing and Technology R&D organization since 2006. Cristina is responsible for specific design tasks of advanced System in Package FC-BGA solutions, mainly focusing on high-end automotive products. She has gained extensive experience in package co-design methodologies and in the planning and definition of complex FC-BGA architecture for system connectivity optimization.

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